



1/49

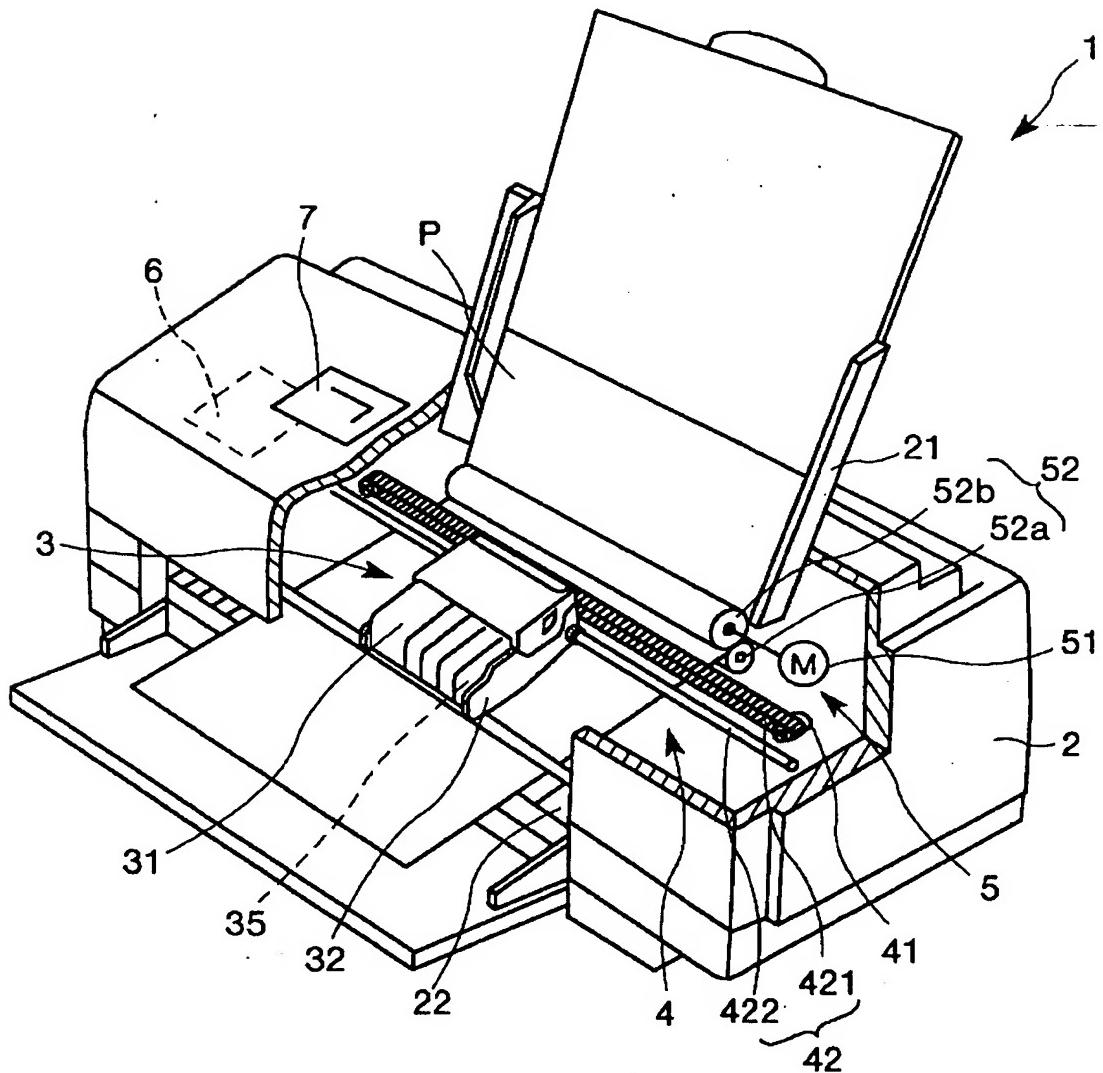


Fig. 1

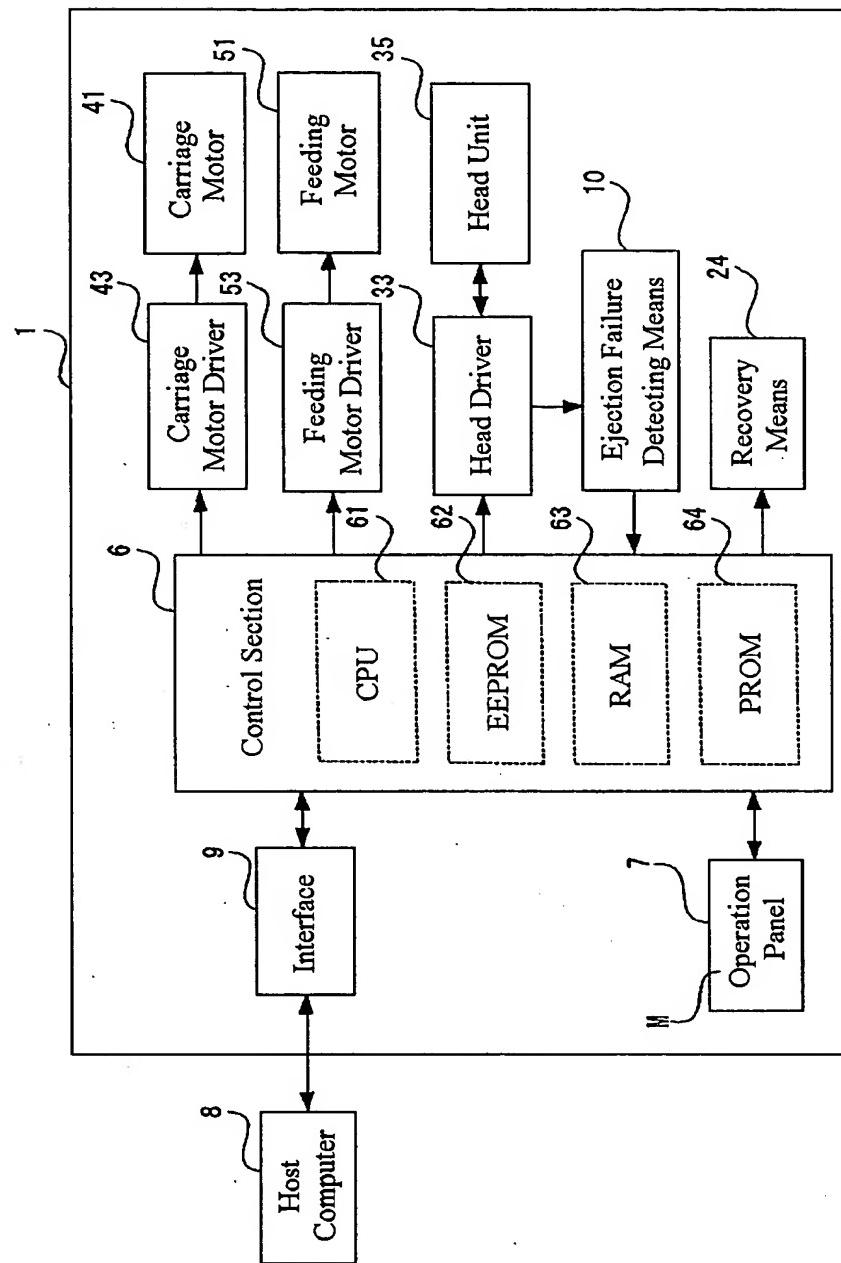


Fig. 2

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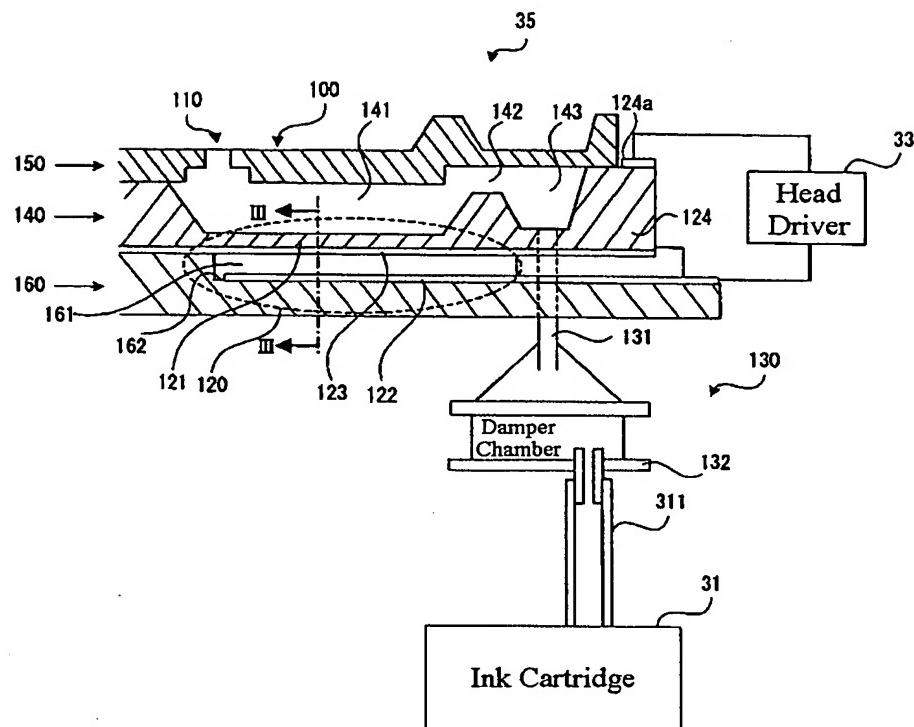


Fig. 3

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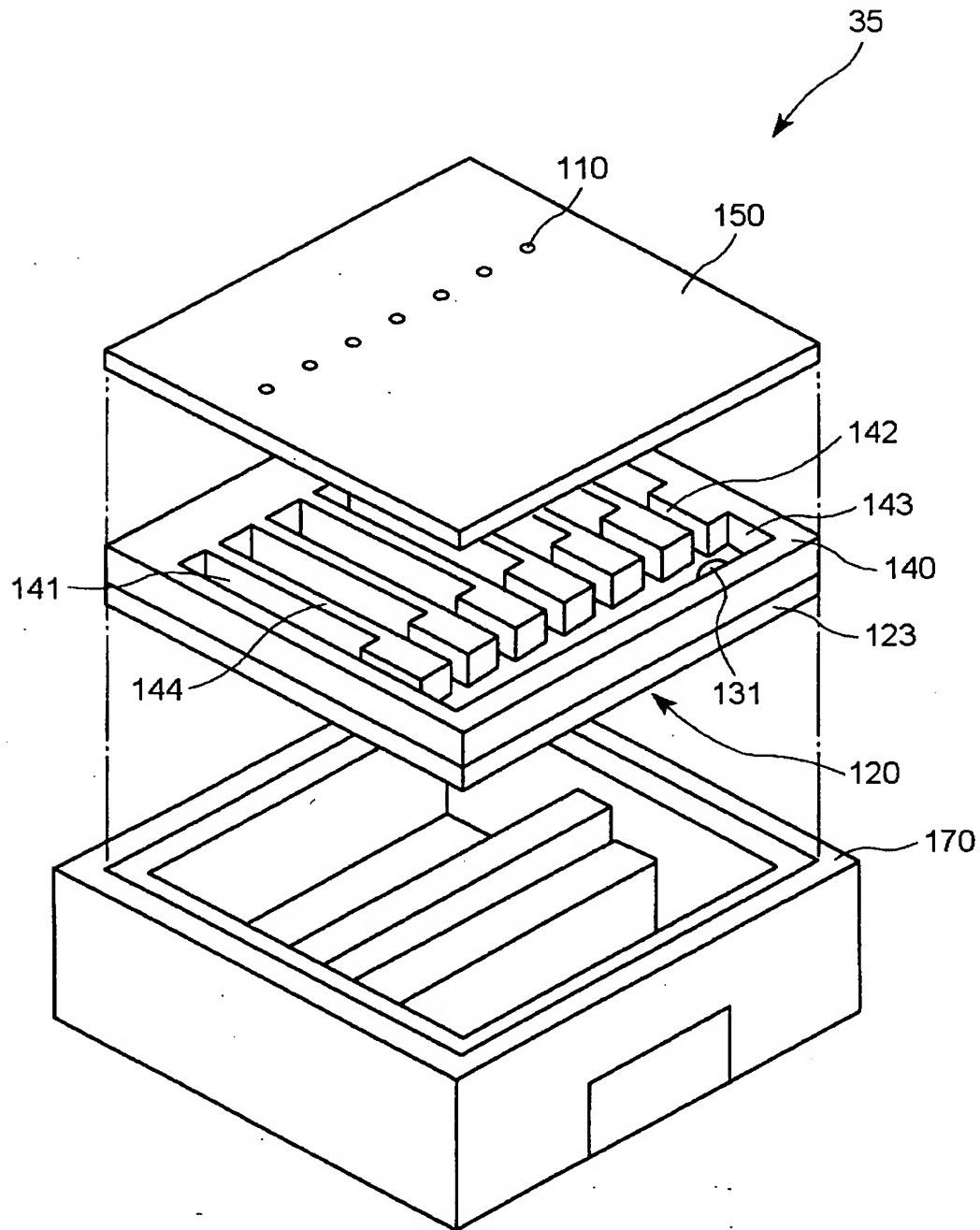


Fig. 4

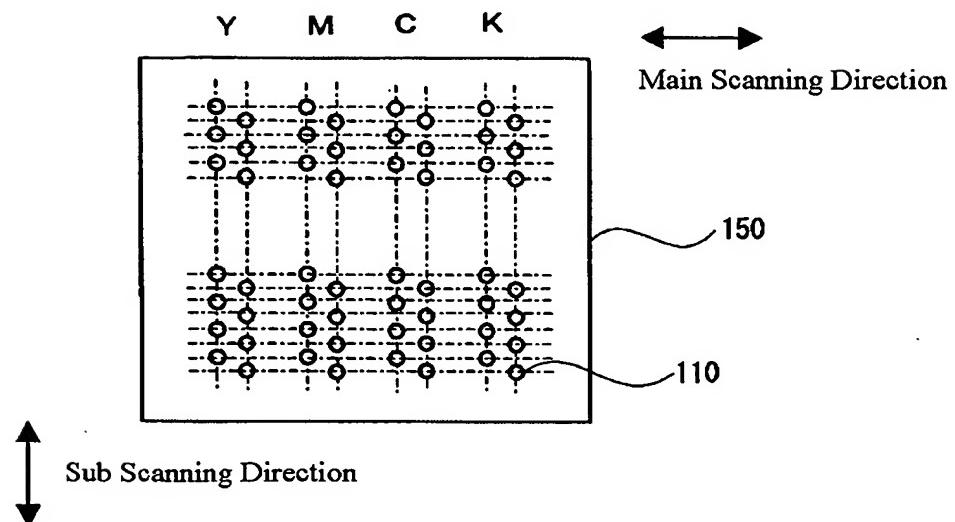


Fig. 5

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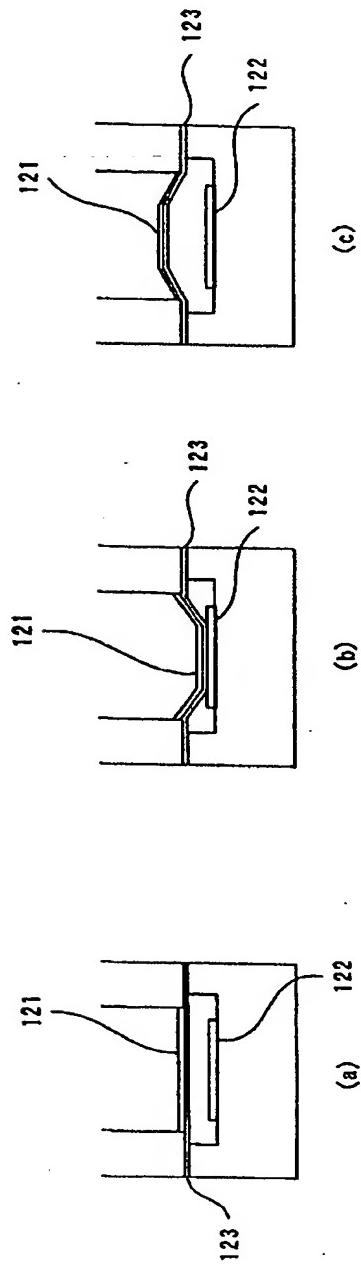


Fig. 6

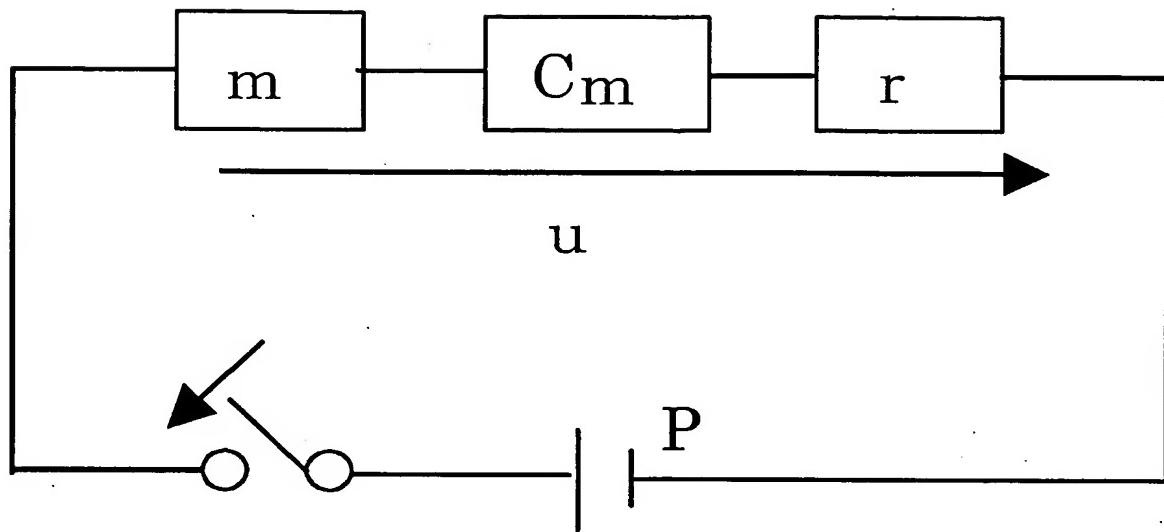


Fig. 7

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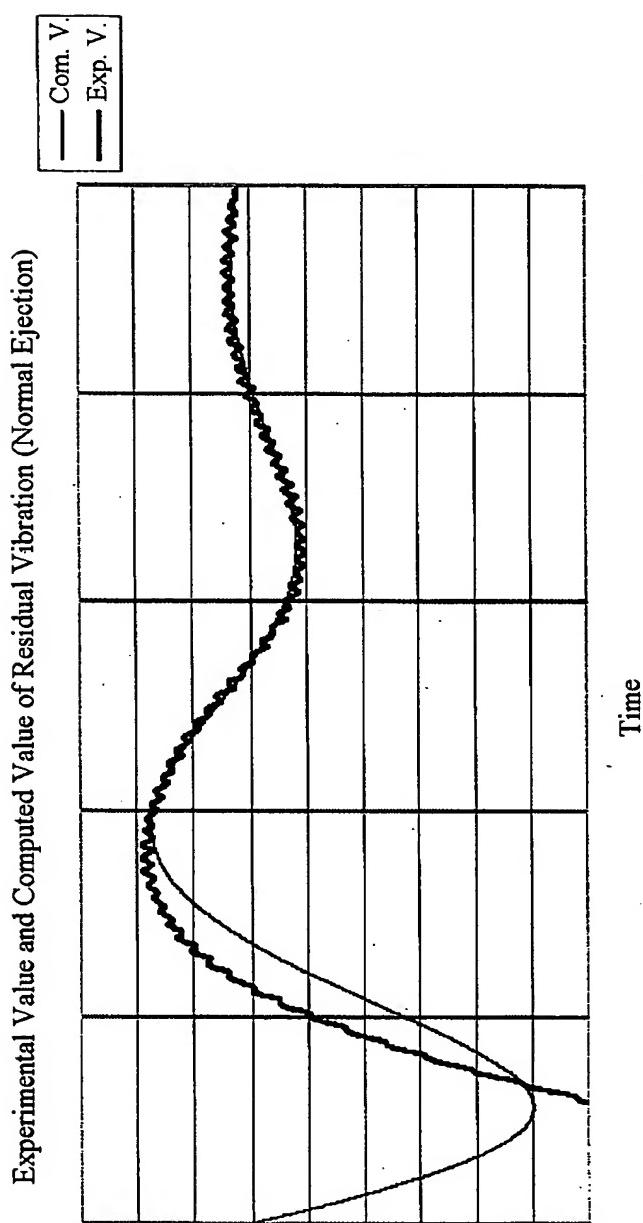


Fig. 8

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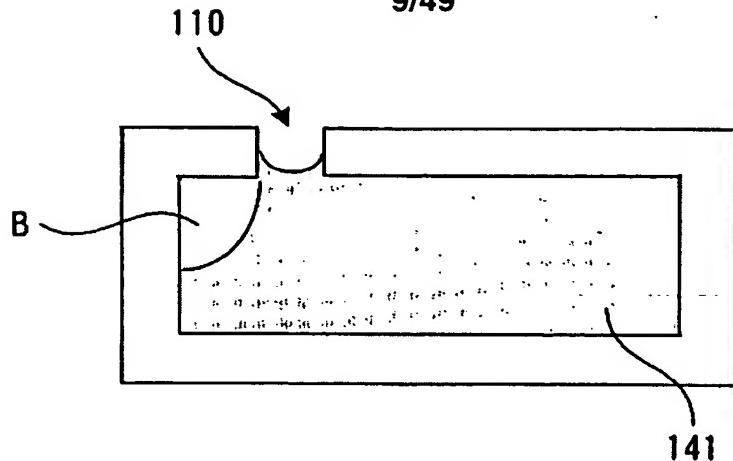


Fig. 9

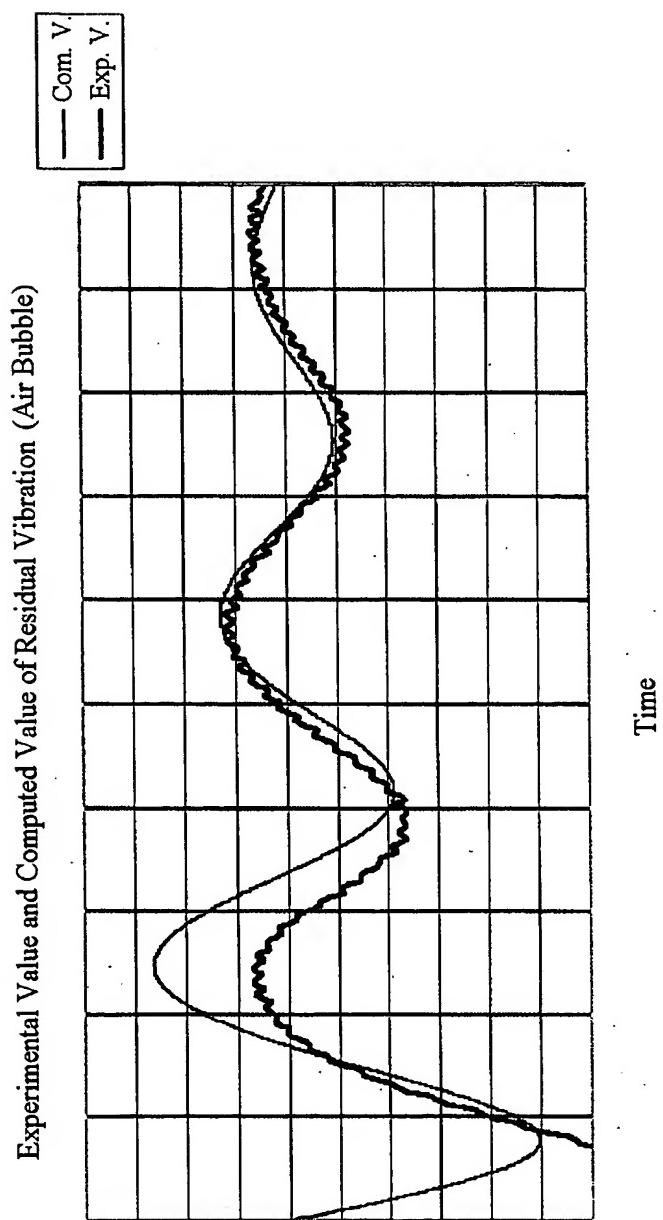


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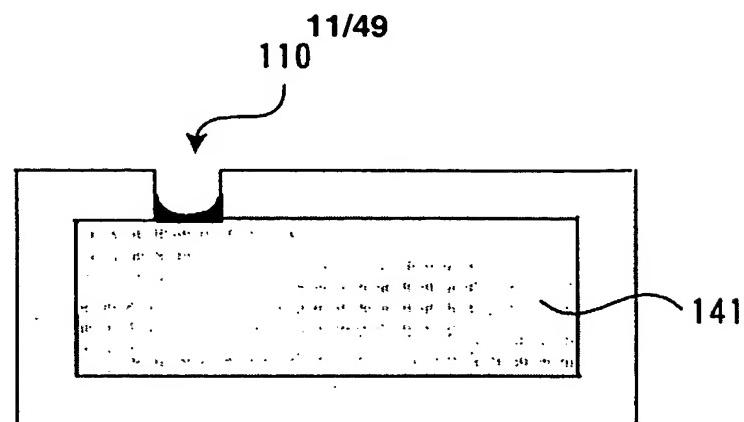


Fig. 11

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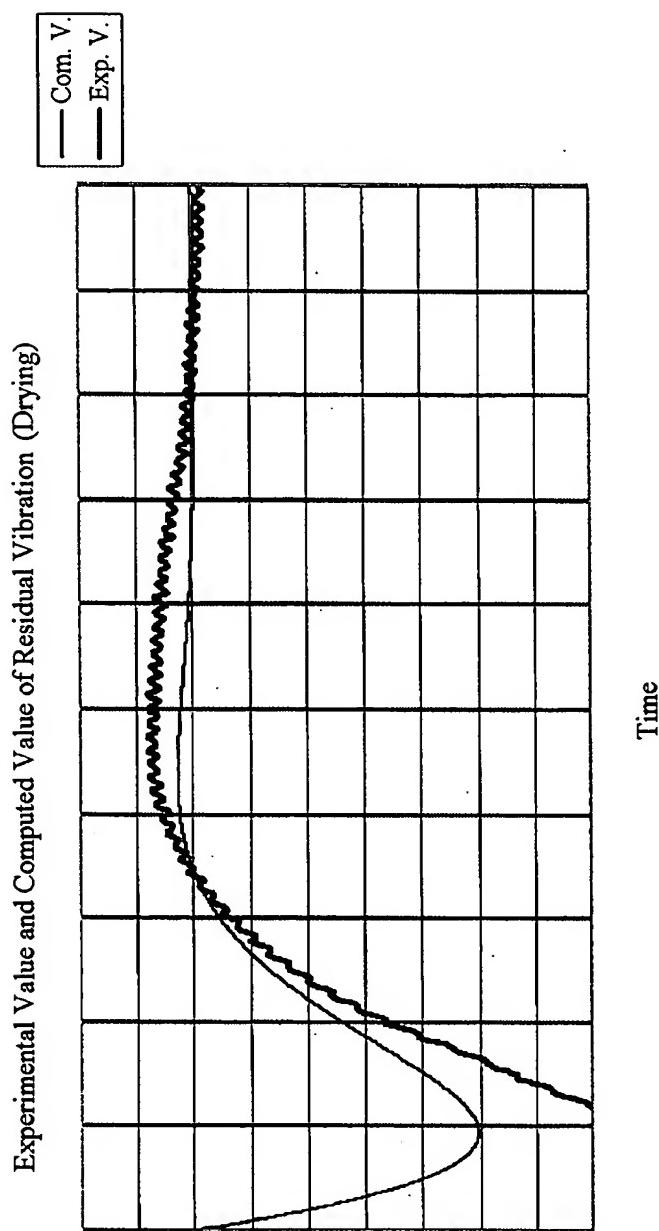


Fig. 12

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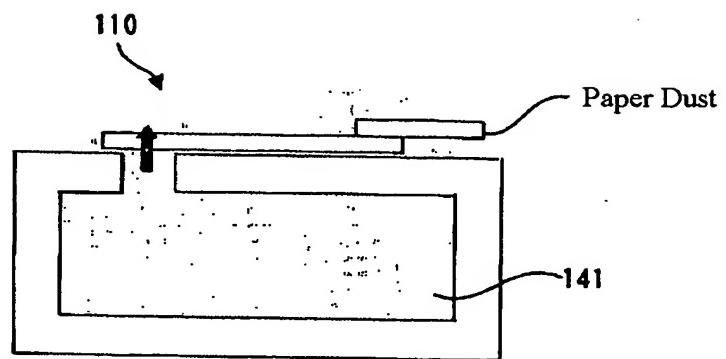


Fig. 13

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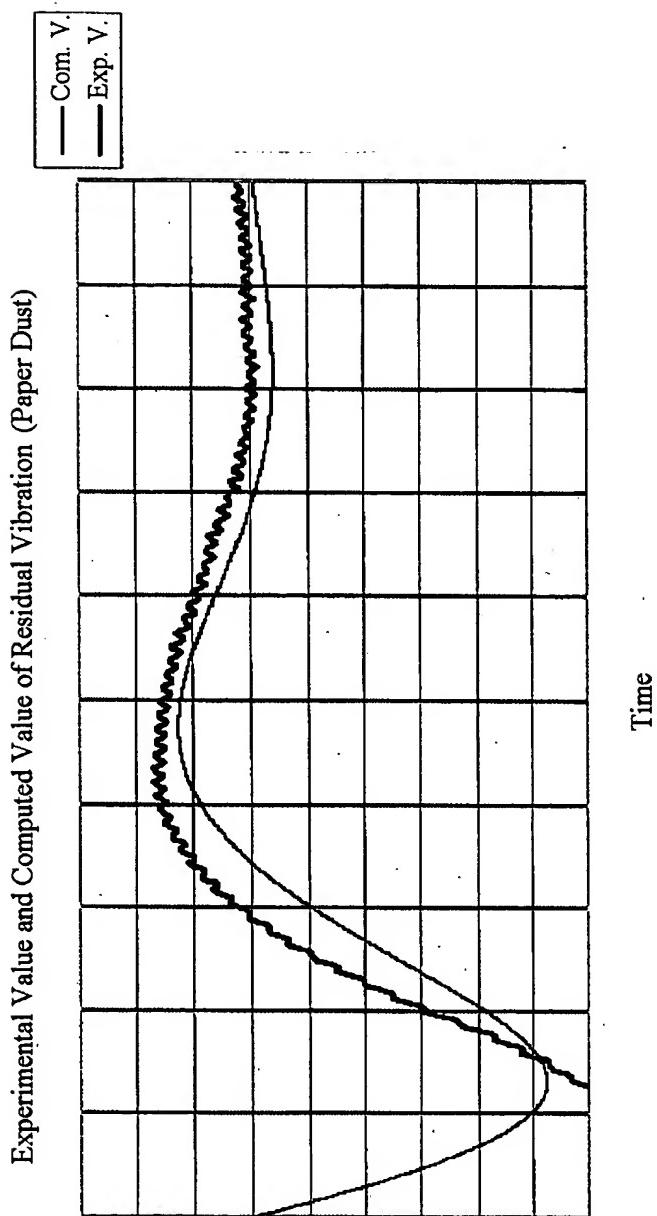


Fig. 14

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Fig. 15

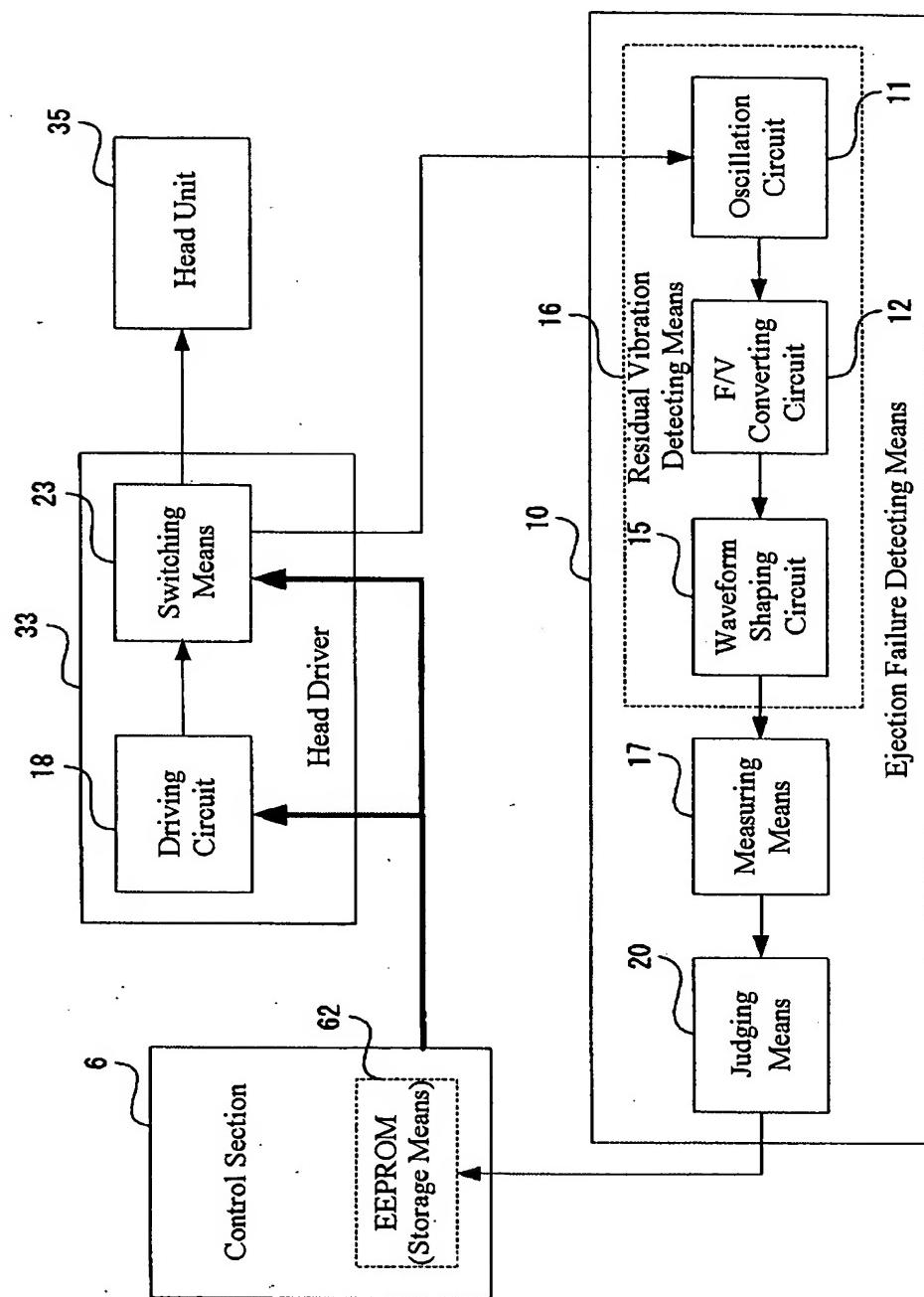


Fig. 16

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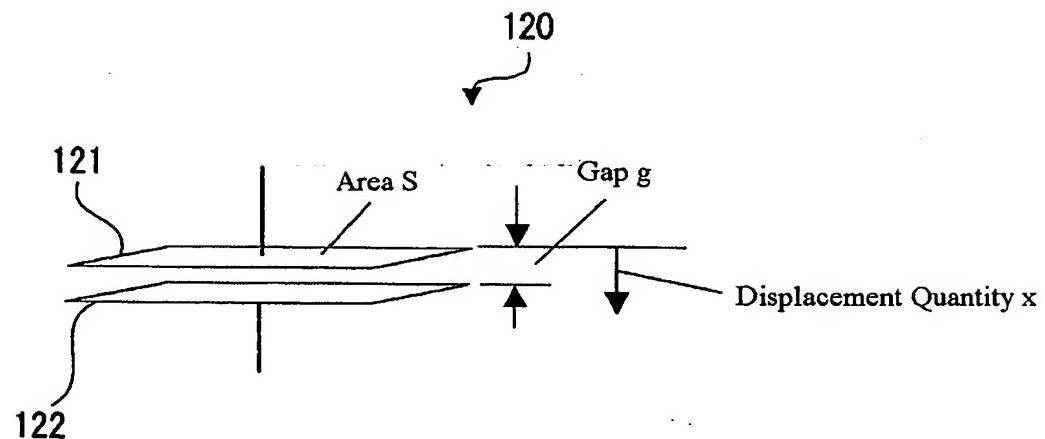


Fig. 17

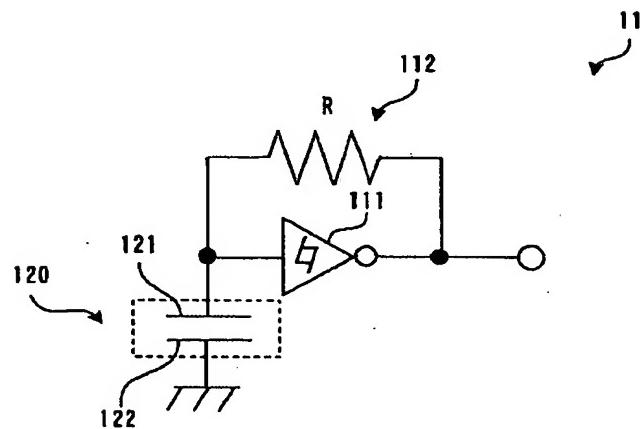


Fig. 18

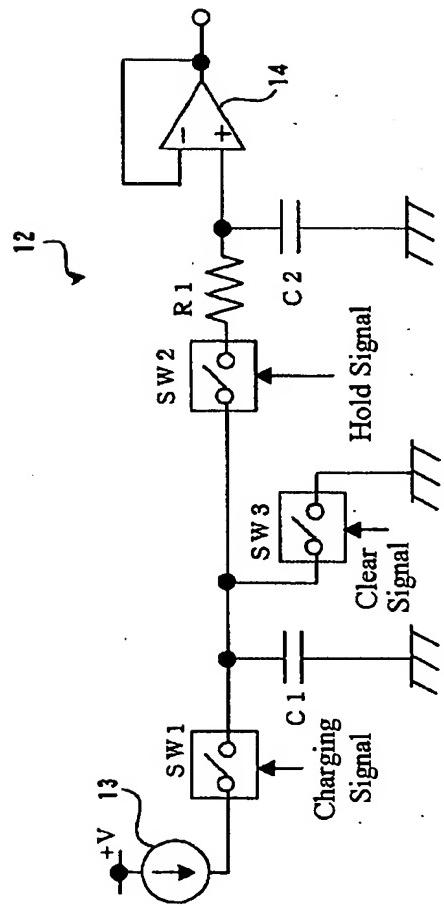


Fig. 19

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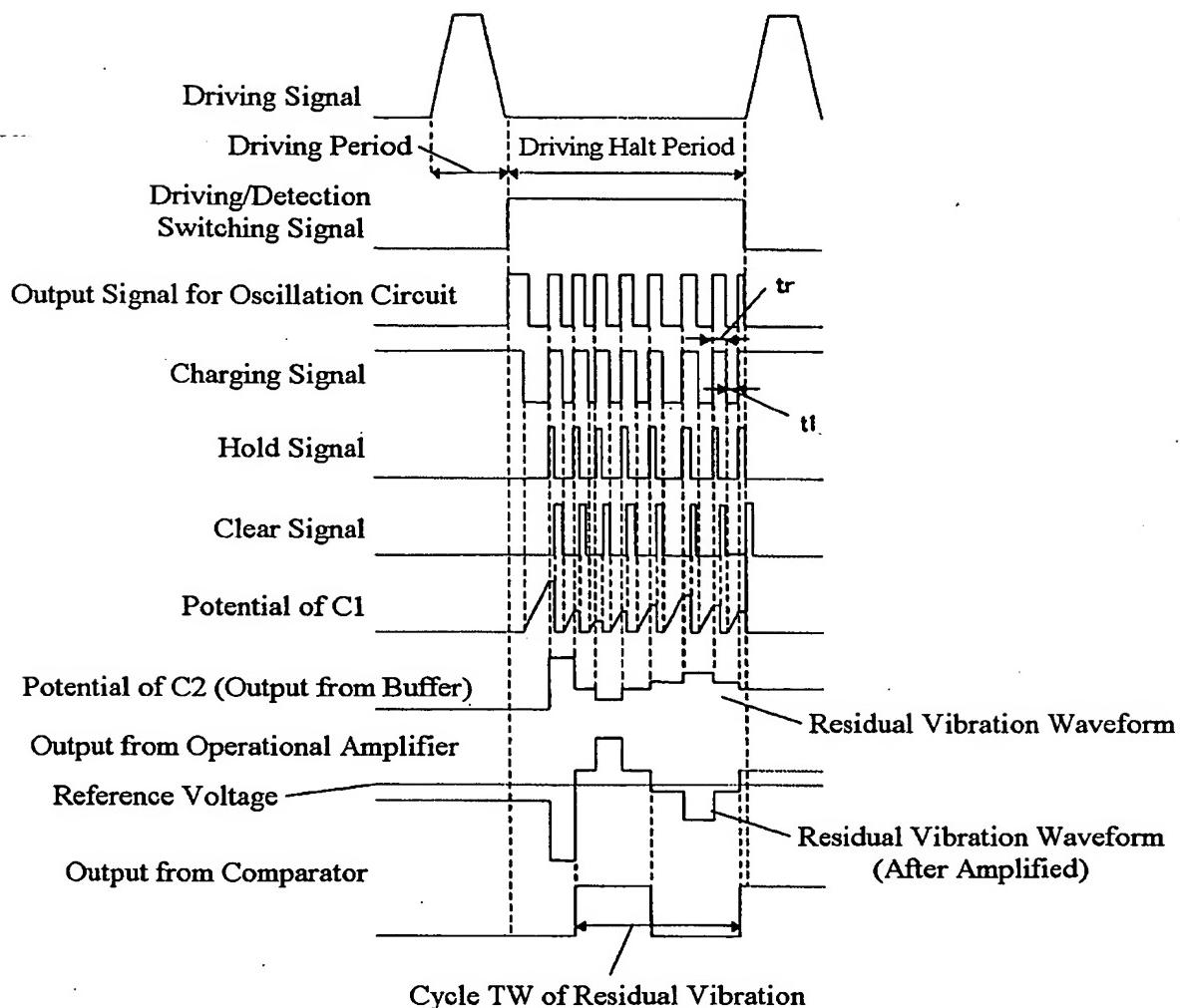


Fig. 20

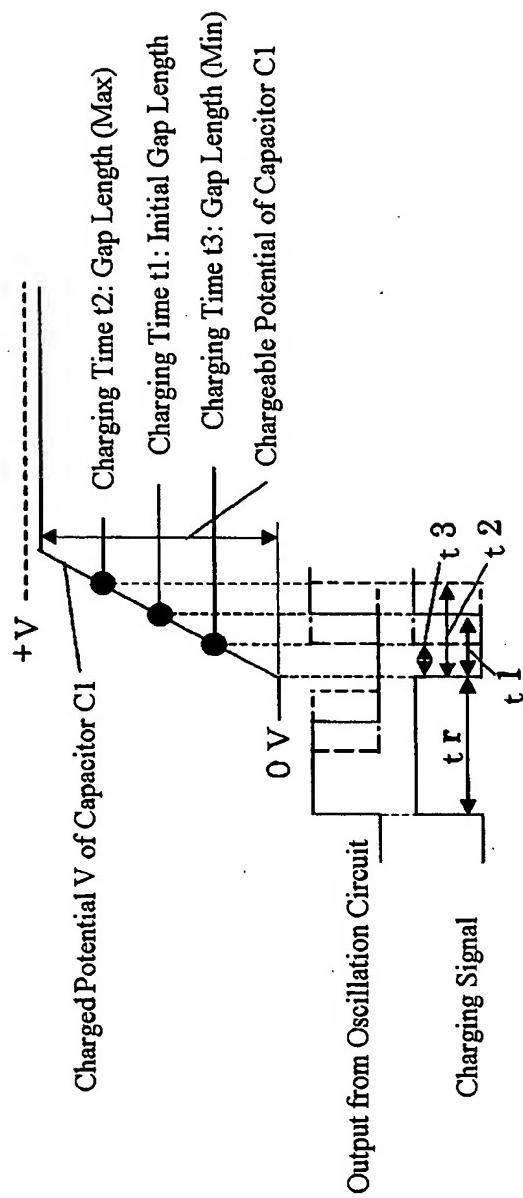


Fig. 21

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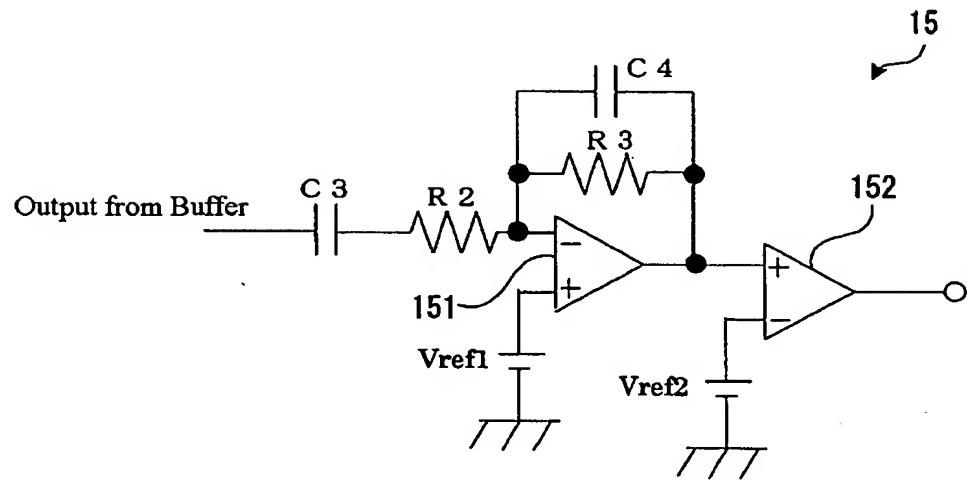


Fig. 22

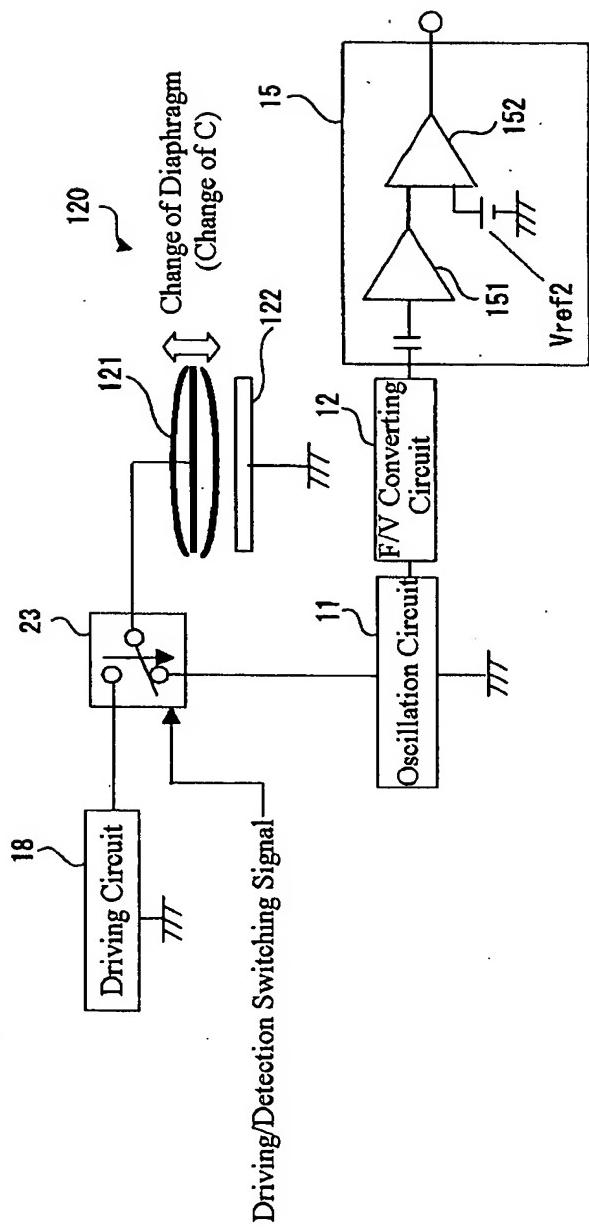


Fig. 23

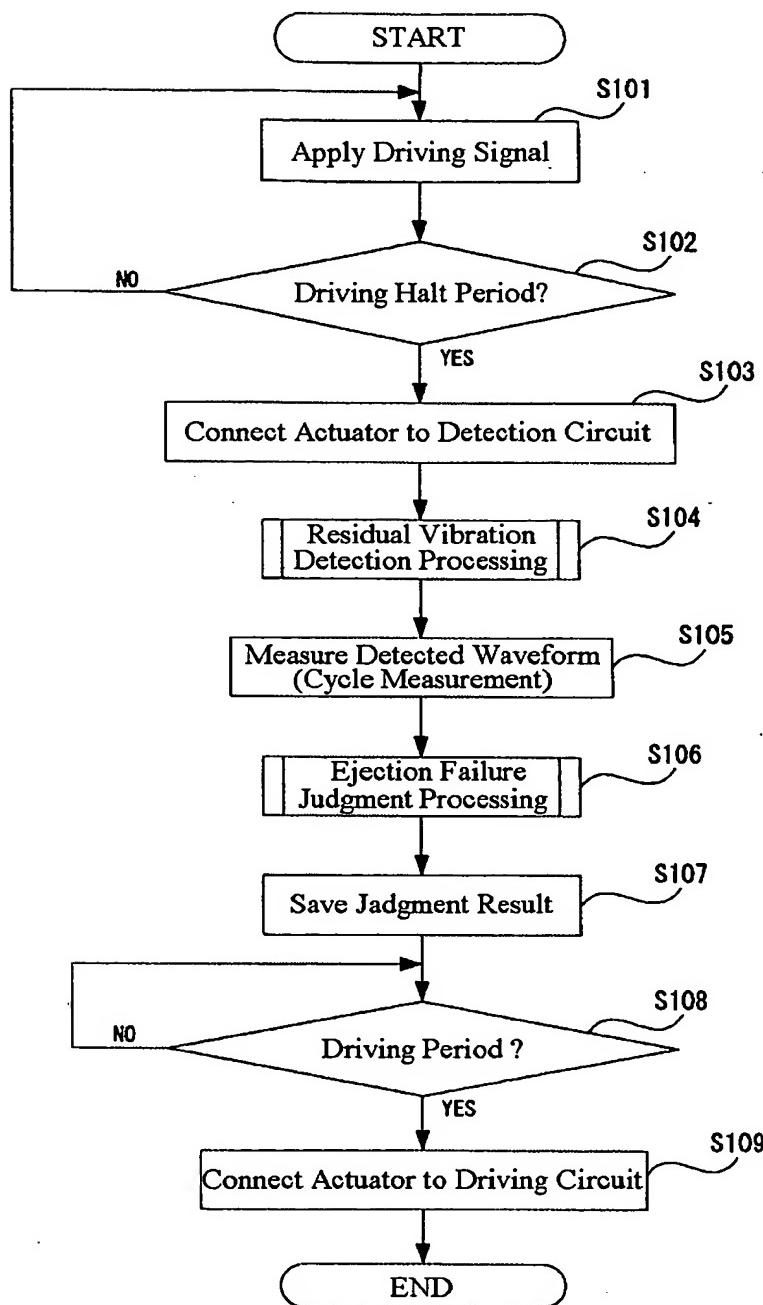


Fig. 24

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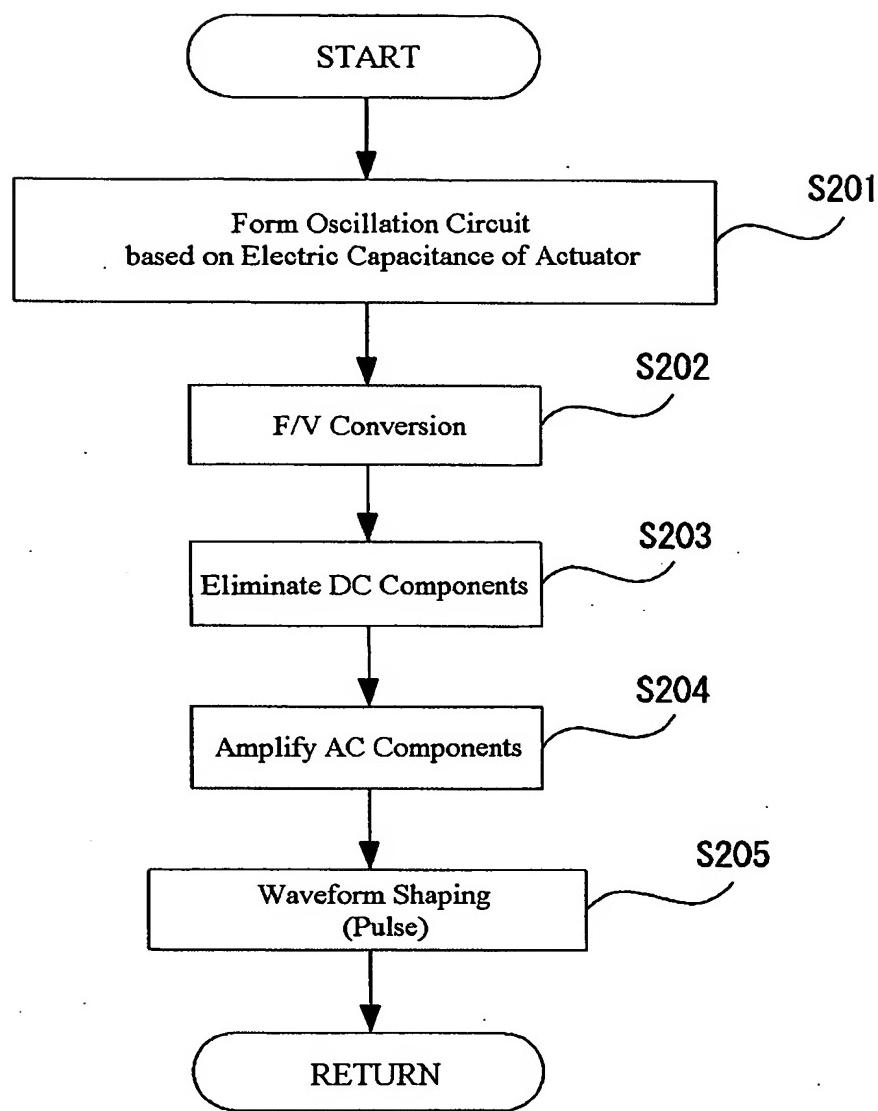


Fig. 25

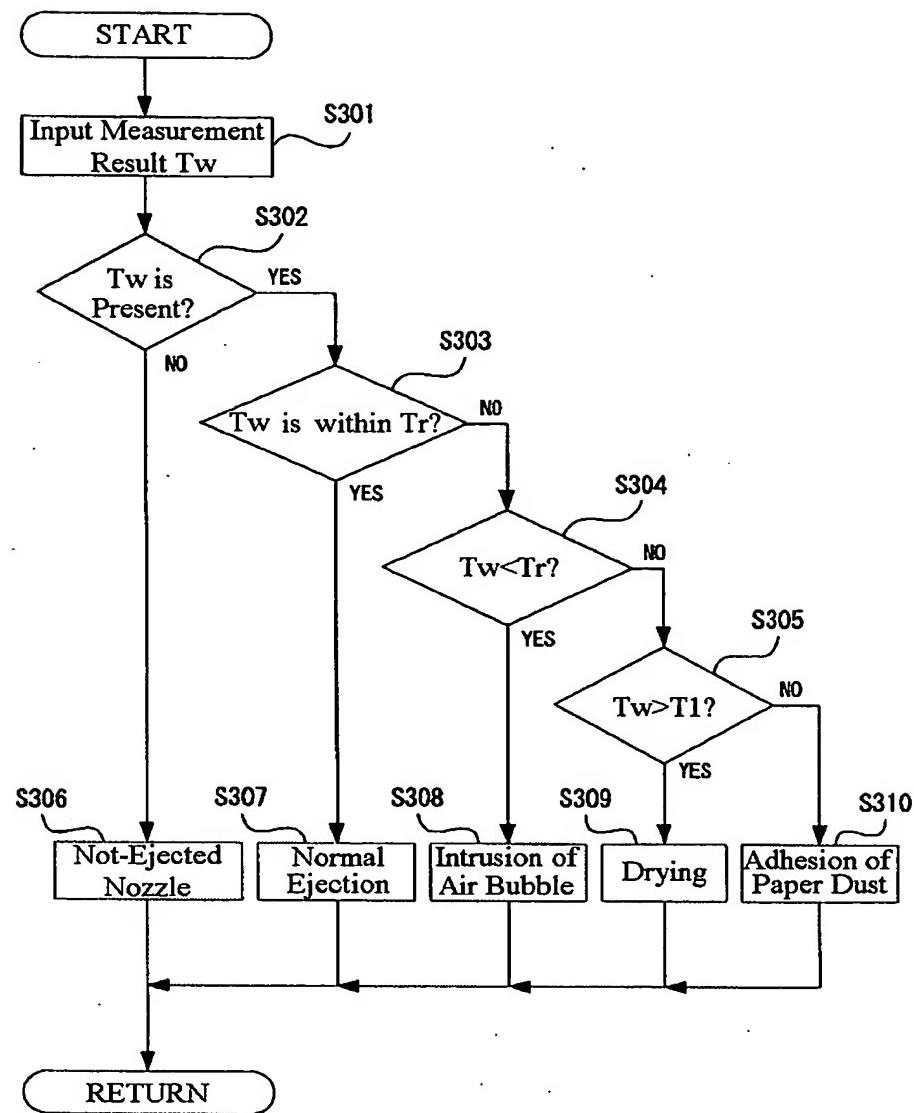


Fig. 26

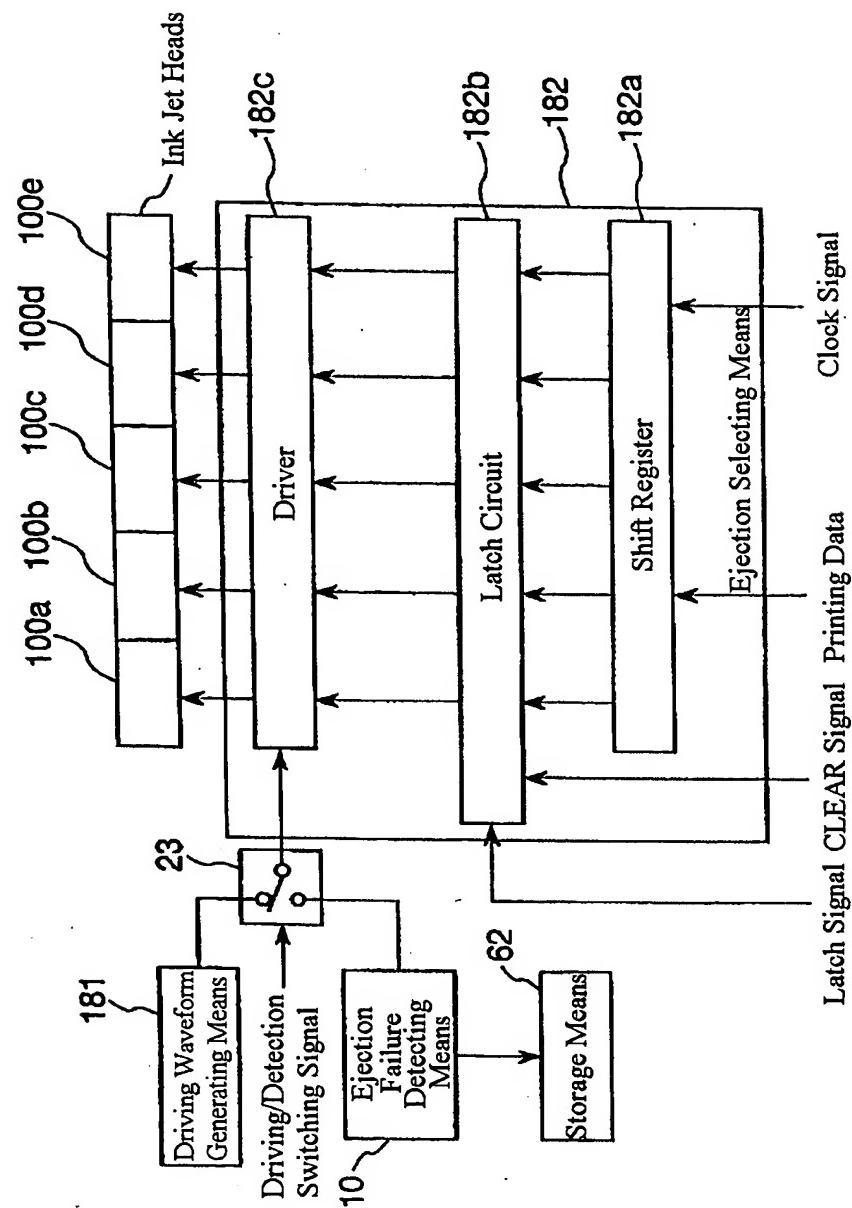


Fig. 27

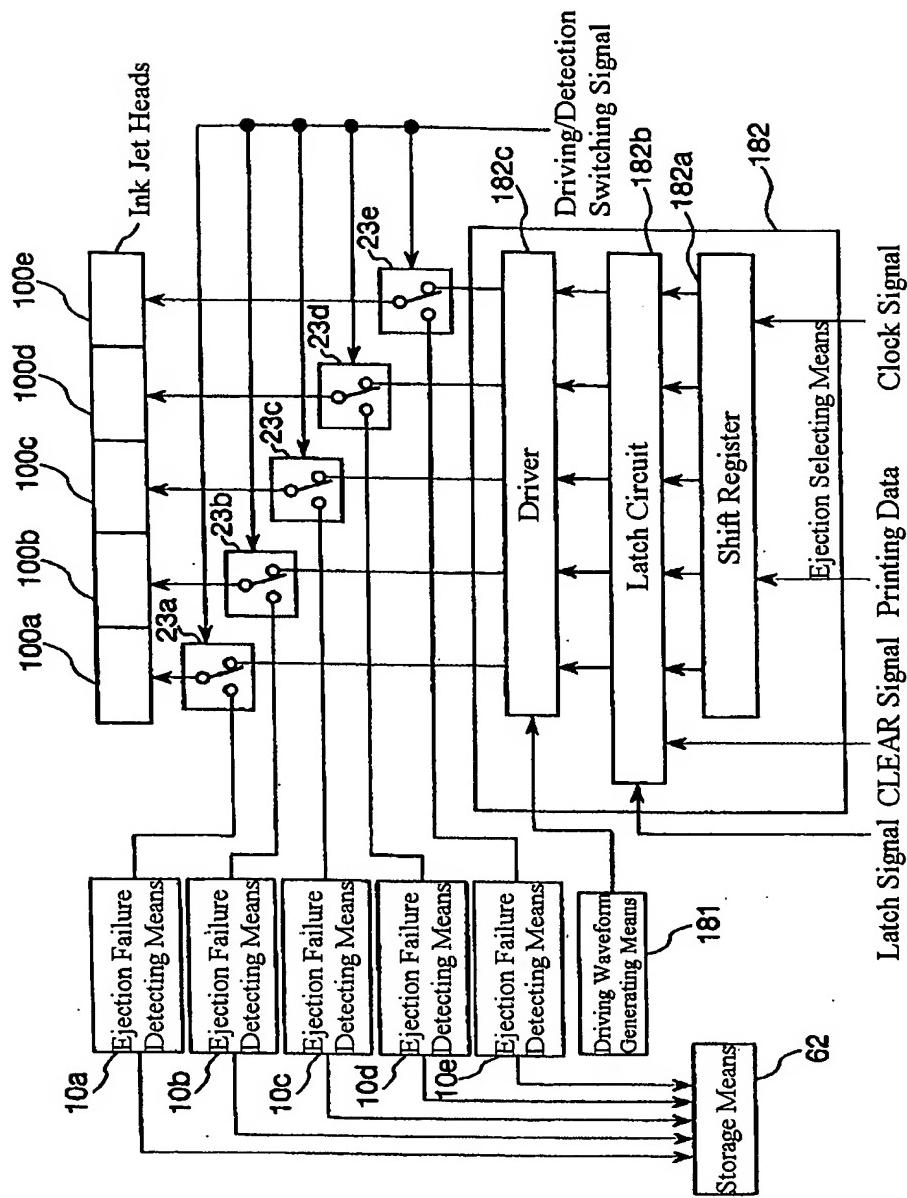


Fig. 28
Latch Signal CLEAR Signal Printing Data Clock Signal

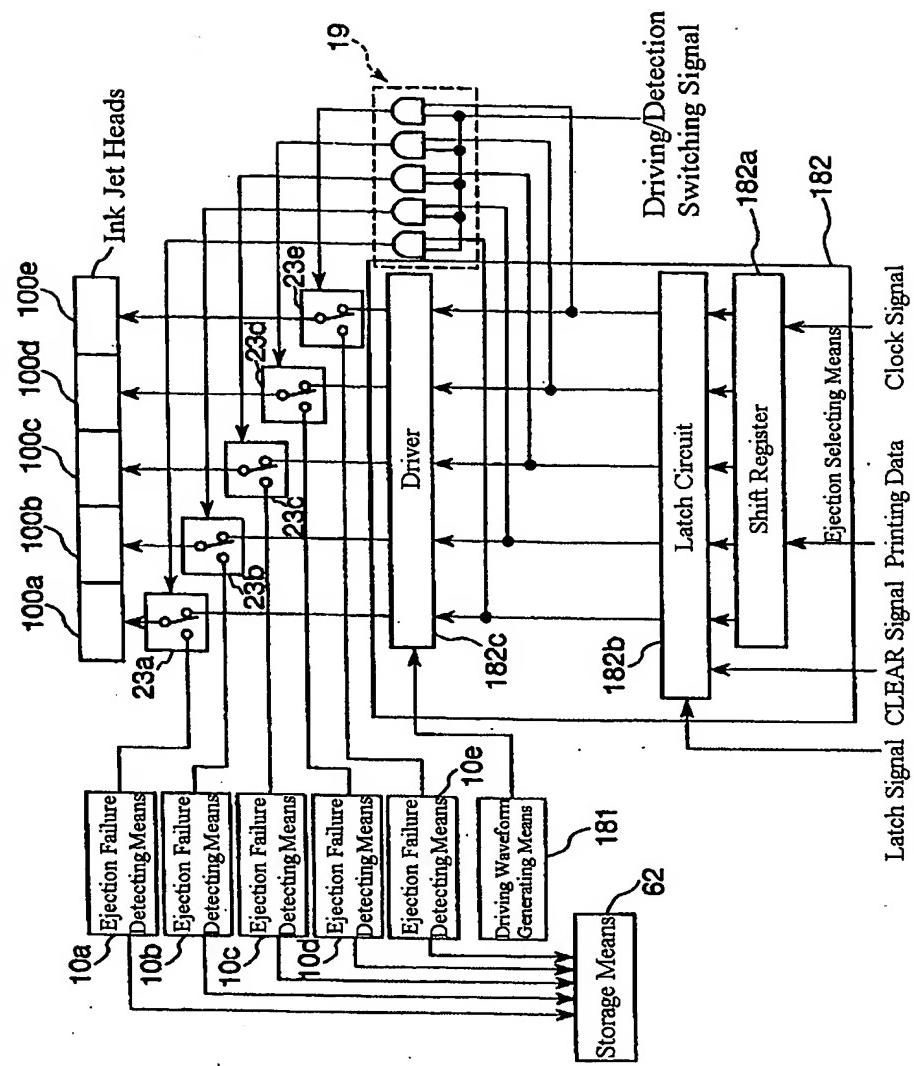


Fig. 29

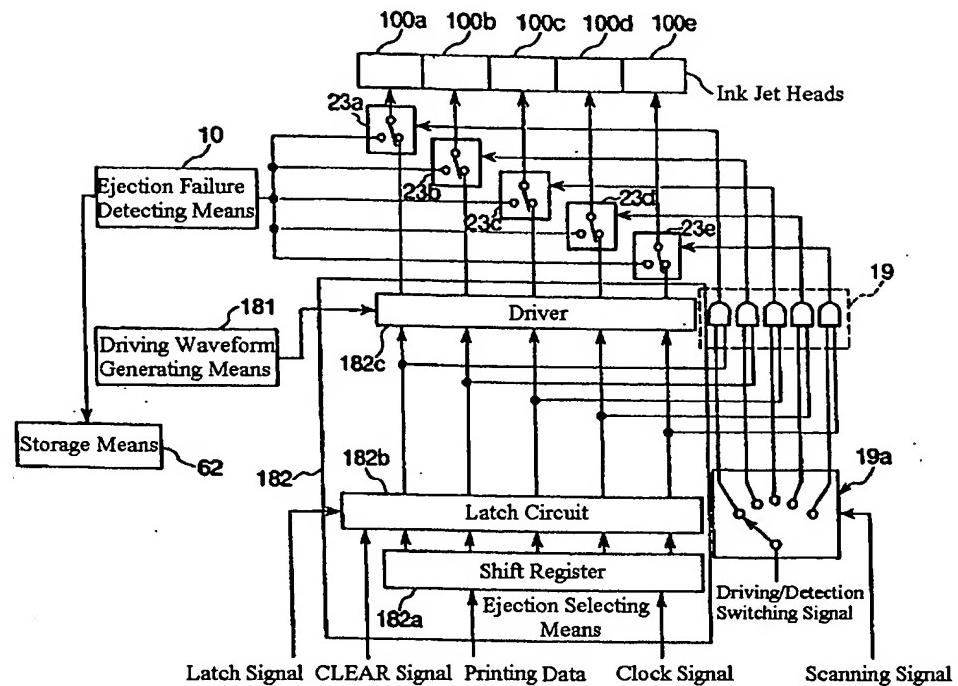


Fig. 30

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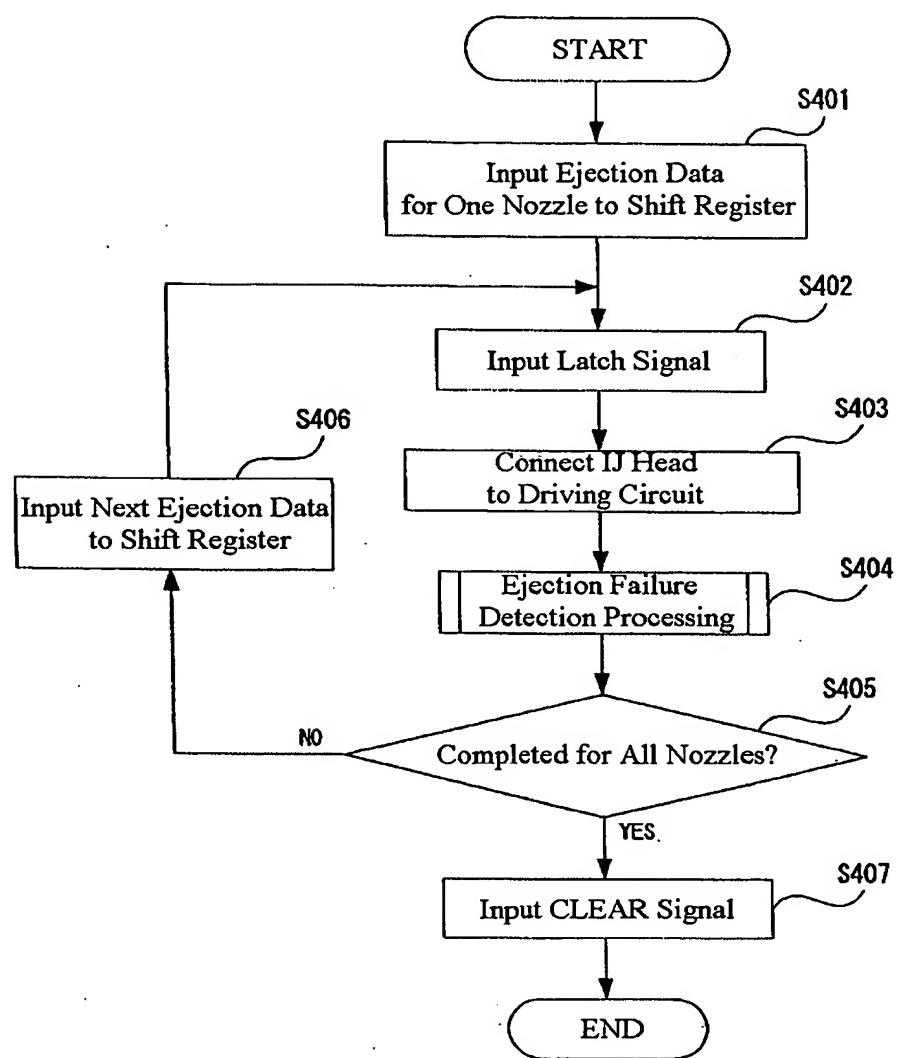


Fig. 31

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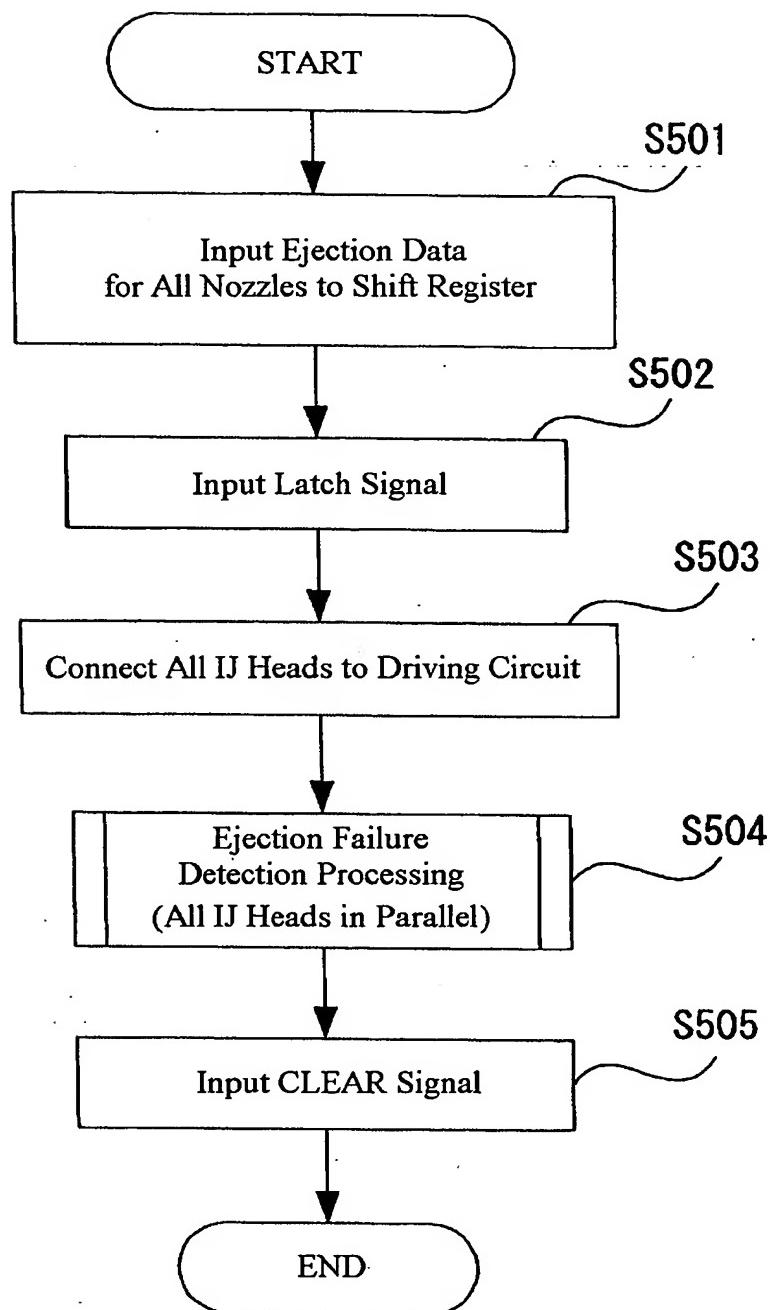


Fig. 32

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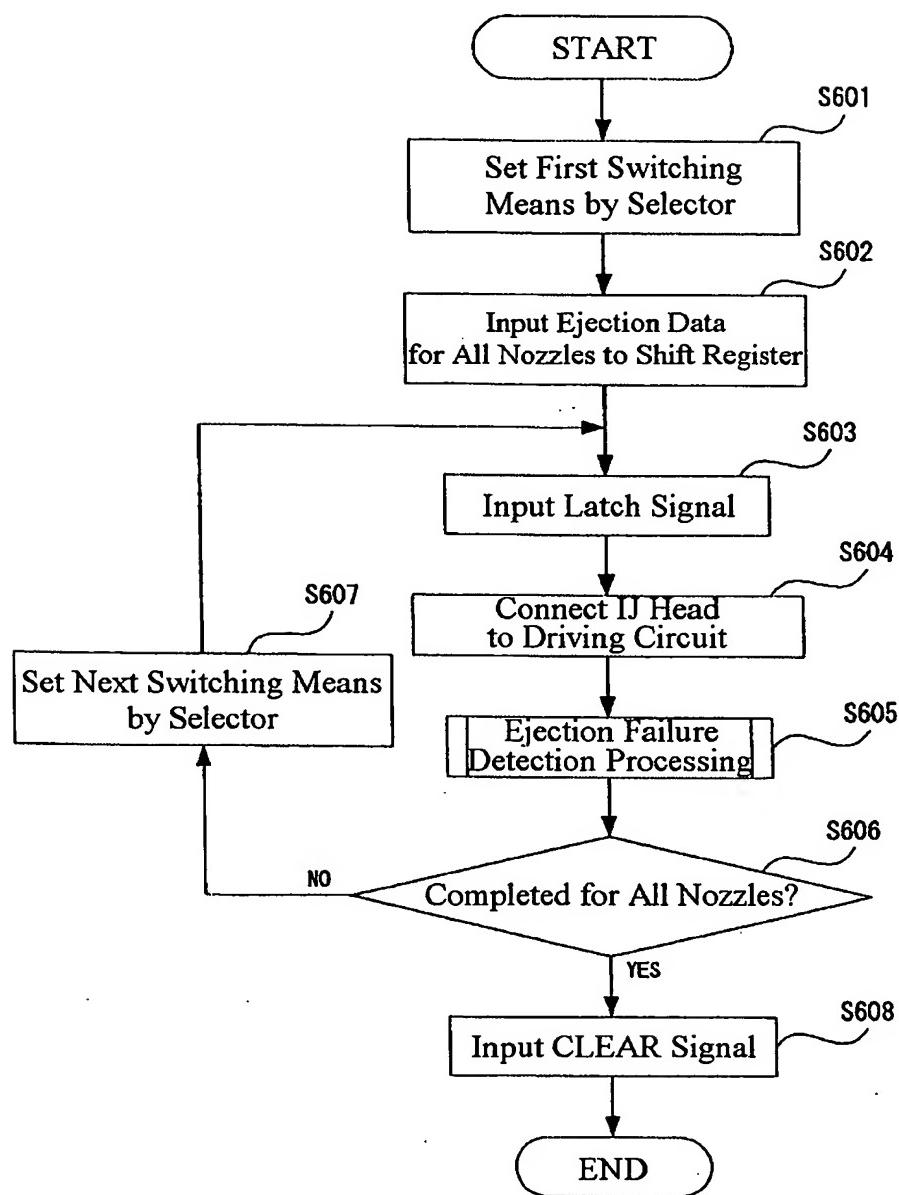


Fig. 33

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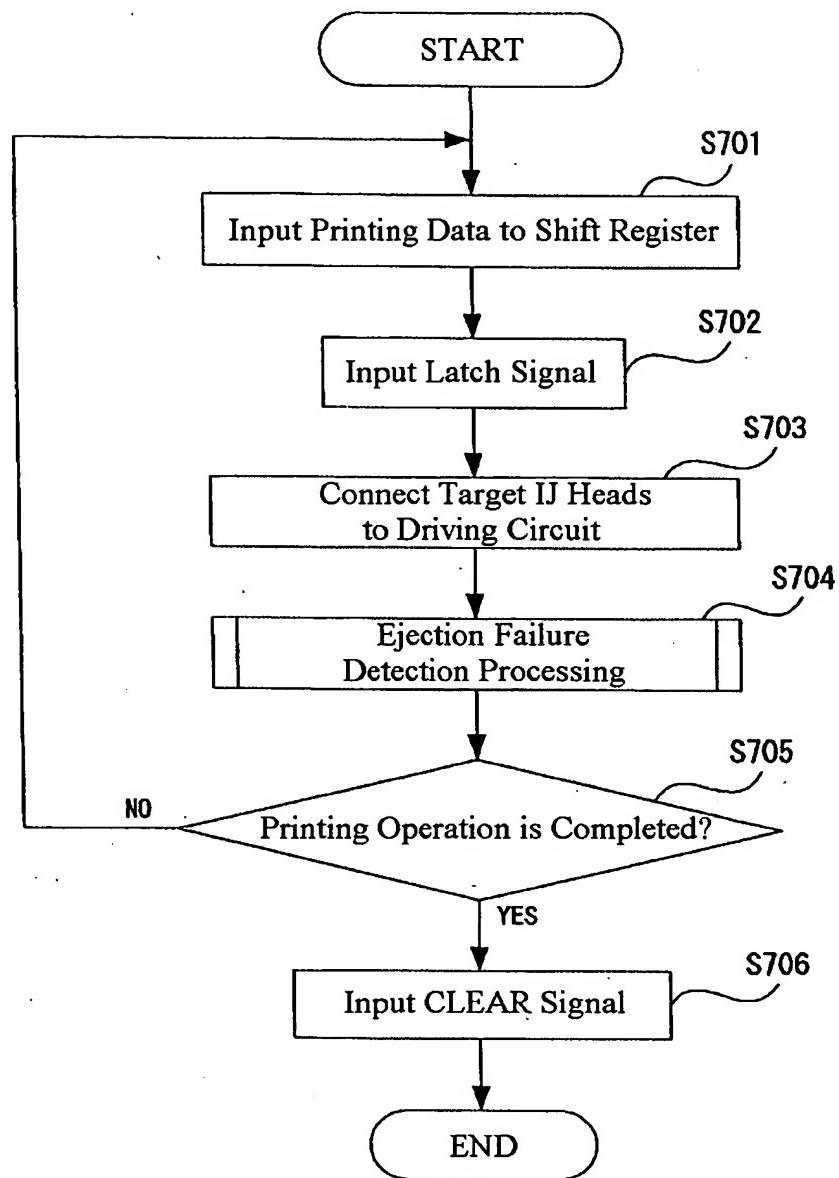


Fig. 34

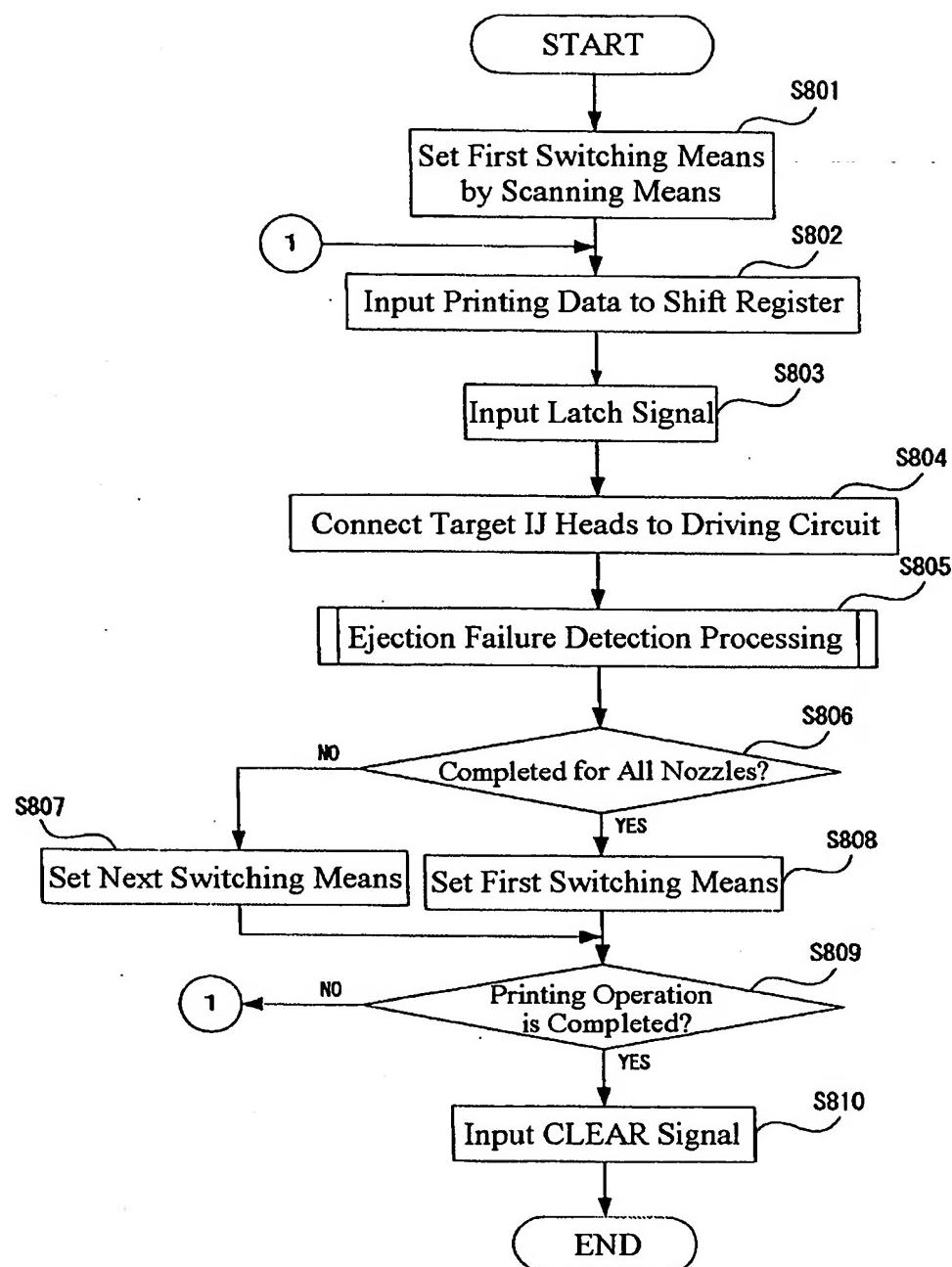


Fig. 35

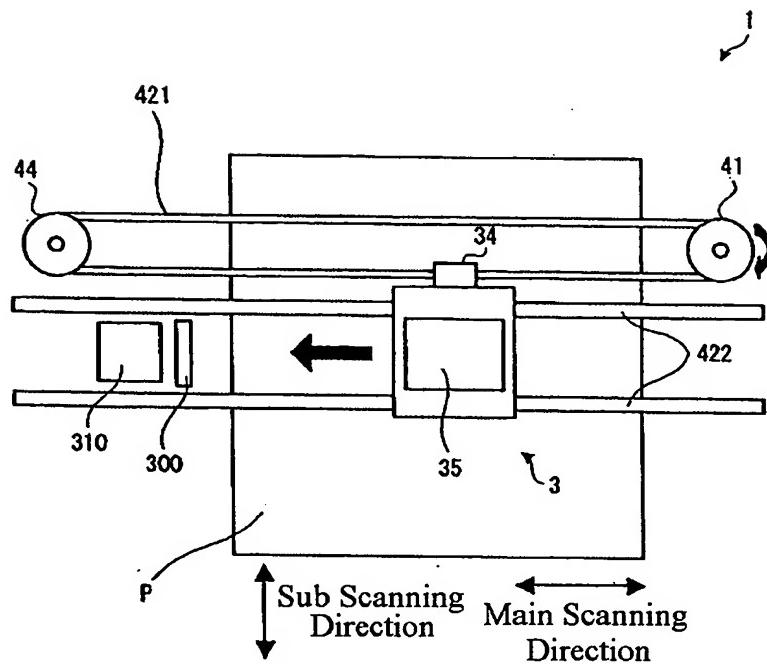


Fig. 36

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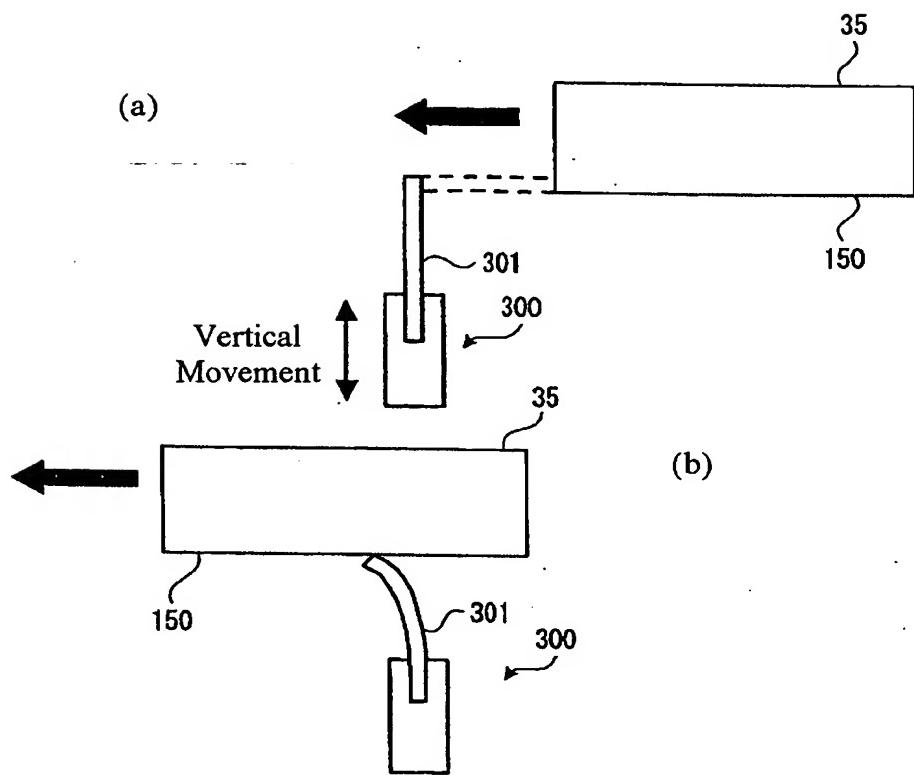


Fig. 37

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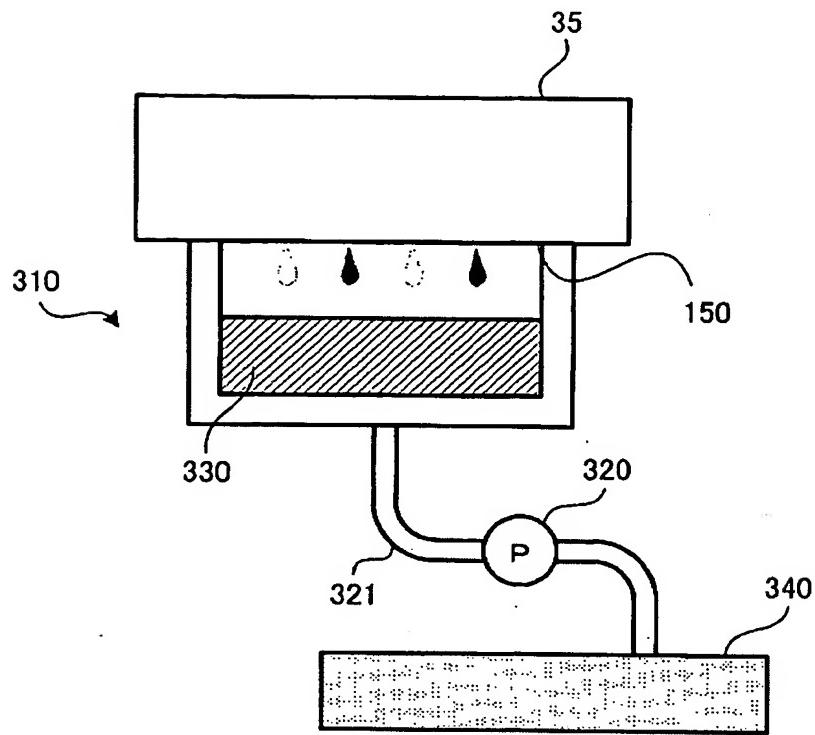


Fig. 38

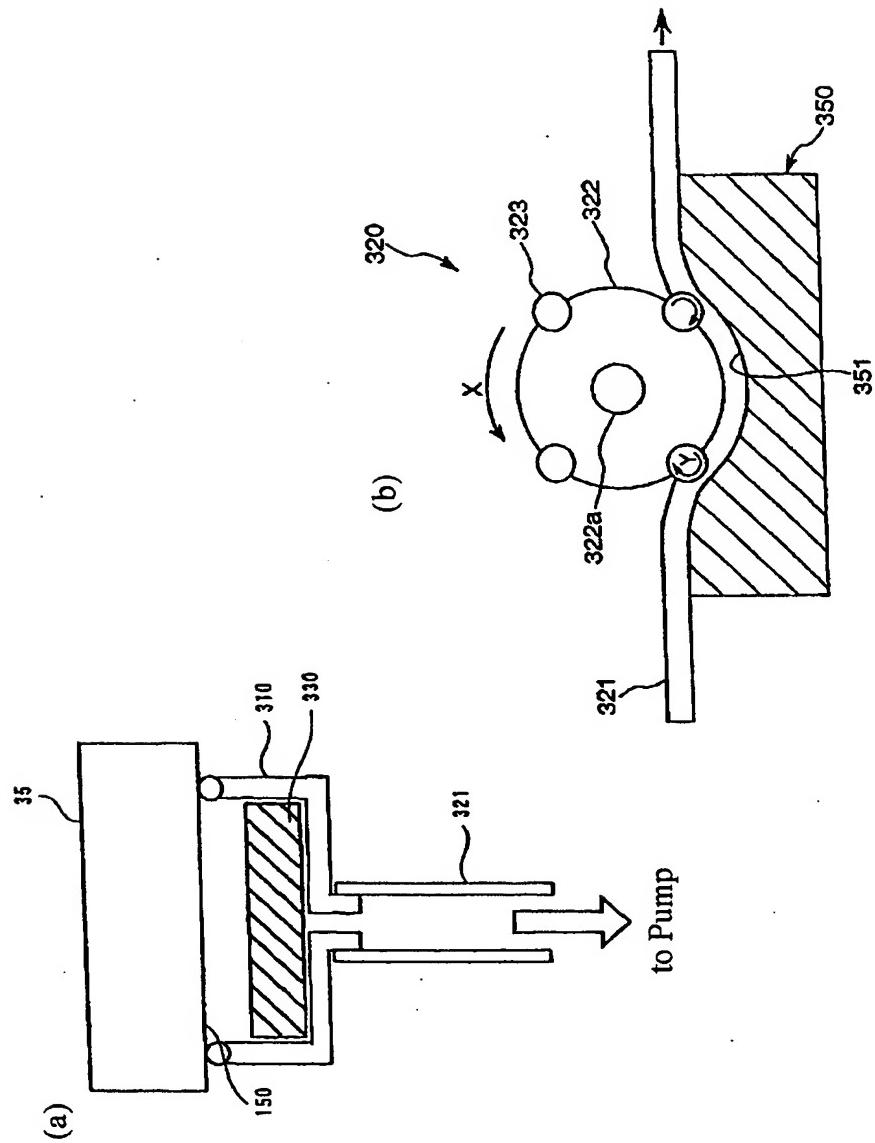


Fig. 39

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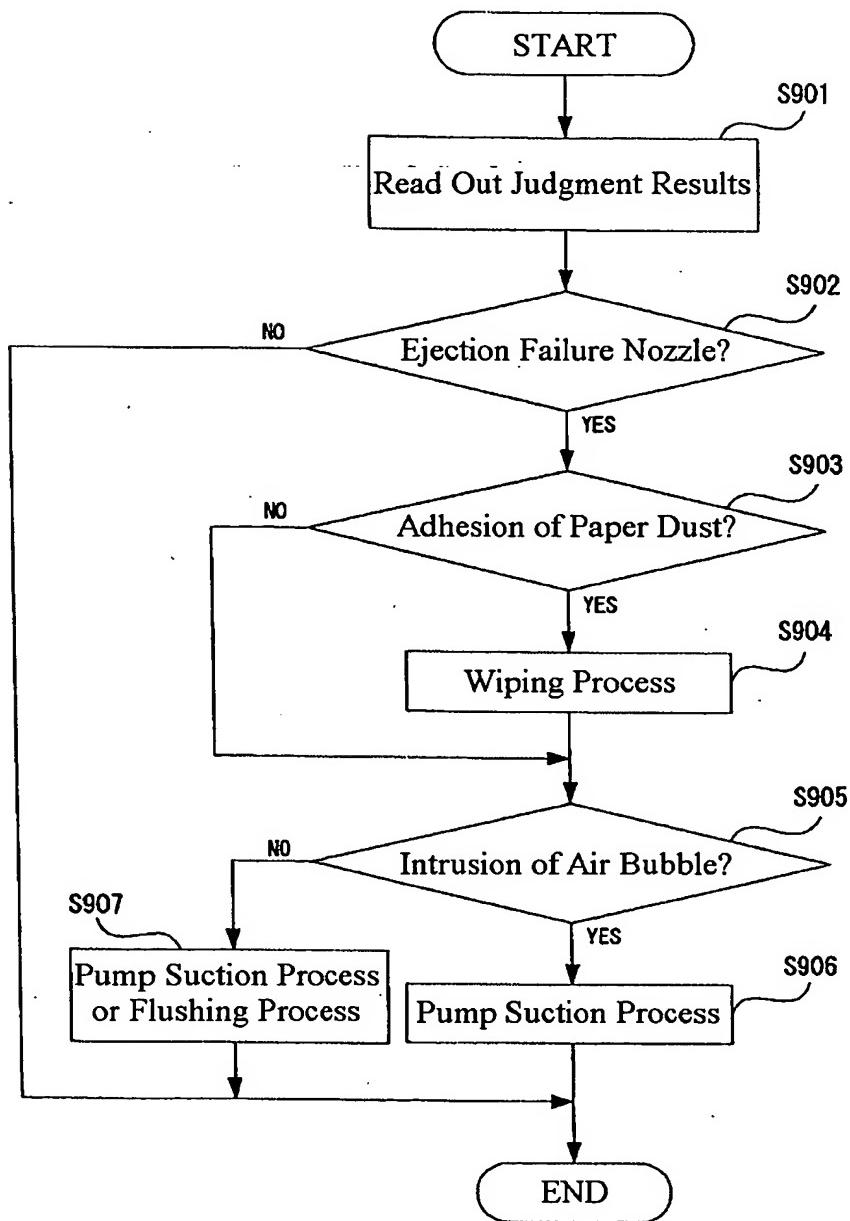


Fig. 40

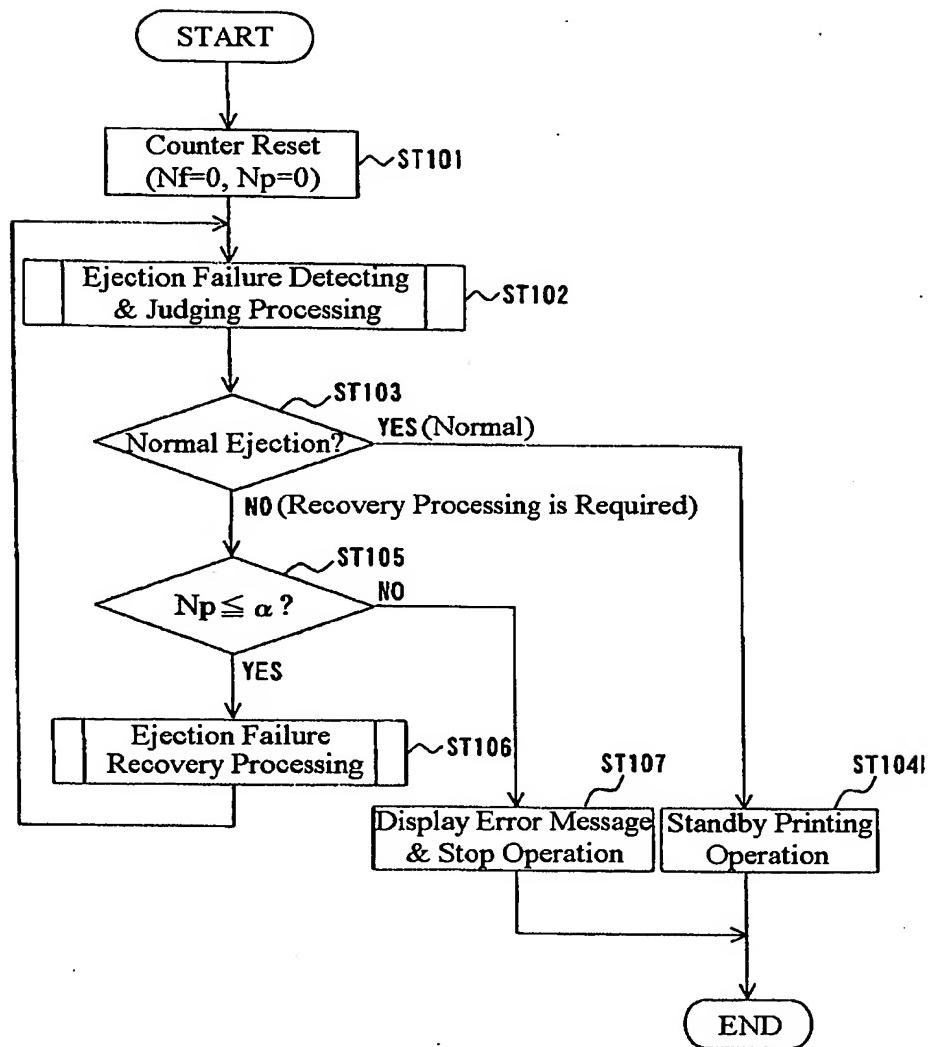


Fig. 41

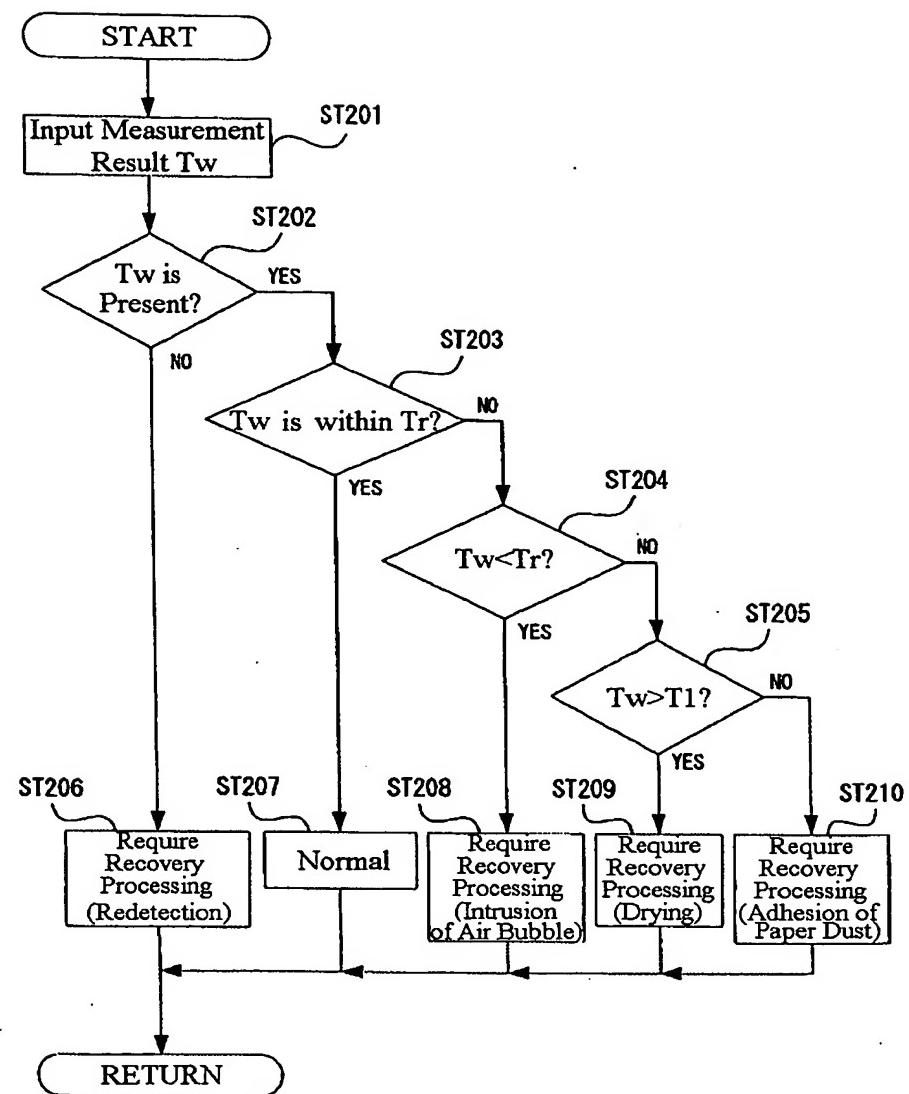


Fig. 42

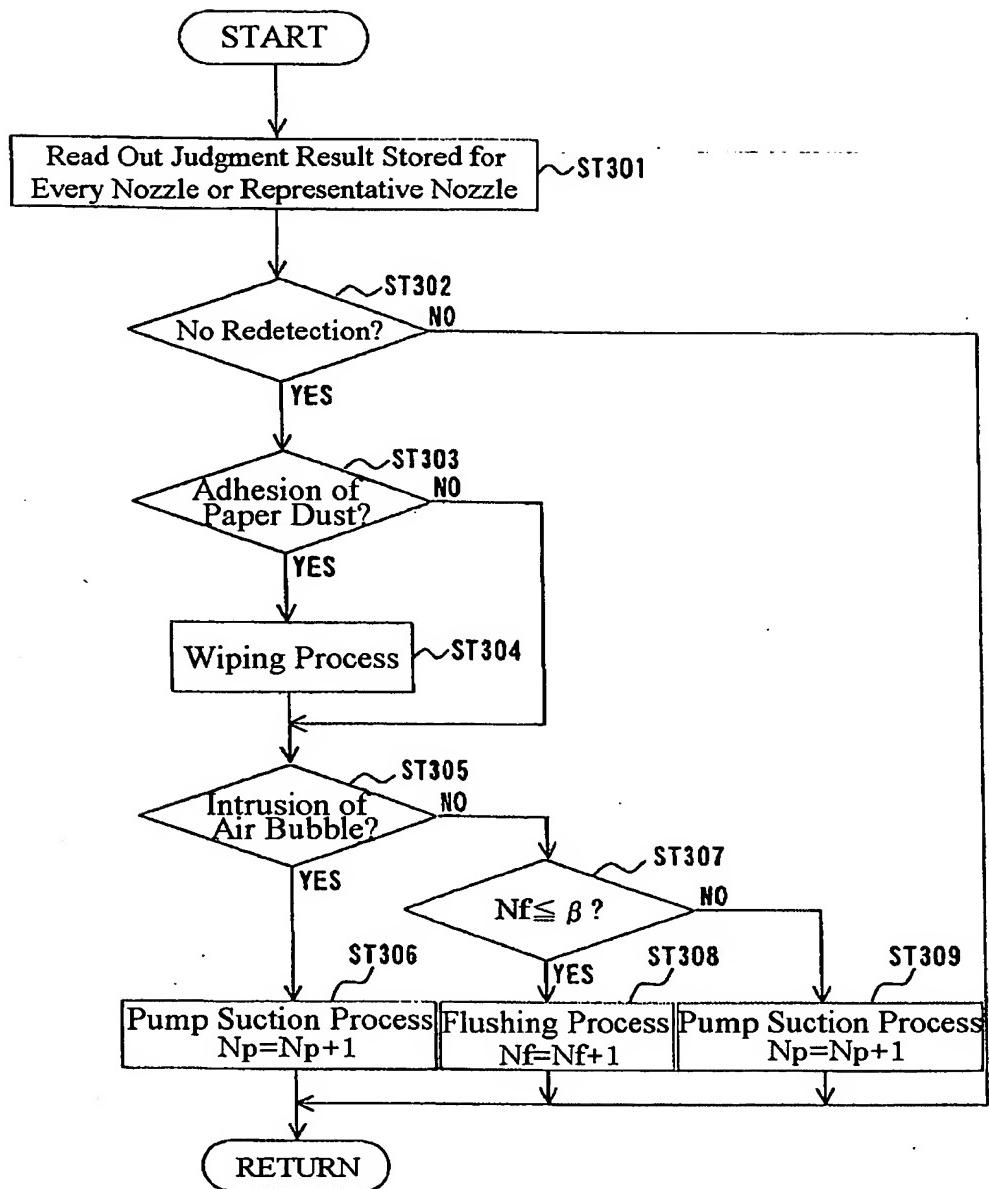


Fig. 43

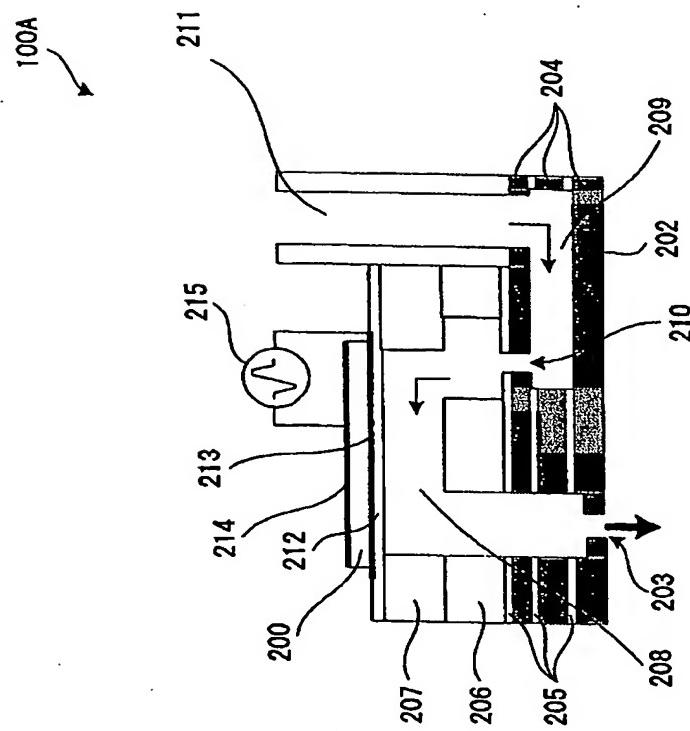


Fig. 44

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100B

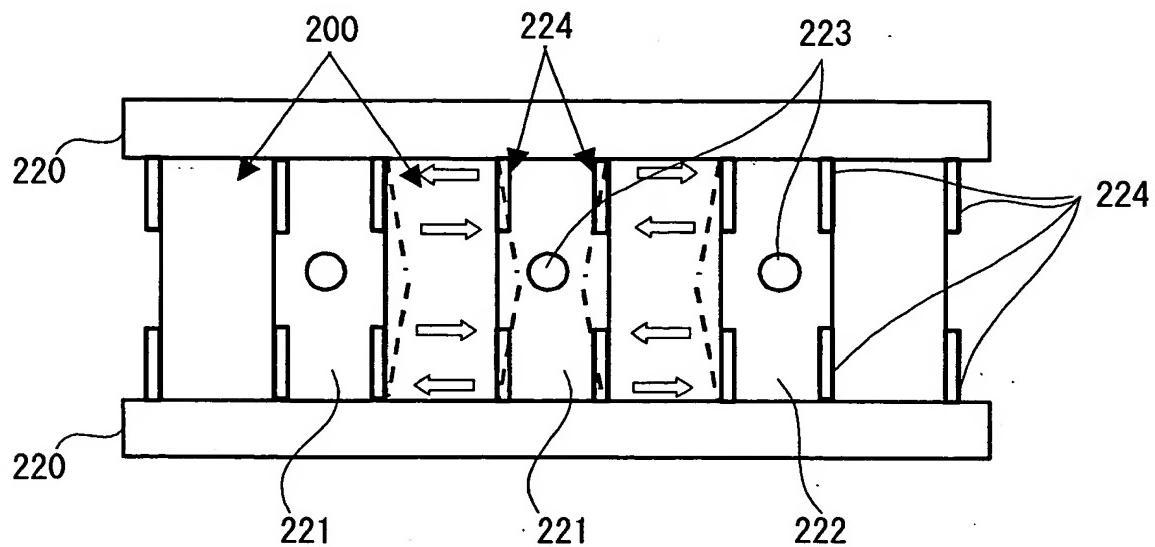


Fig. 45

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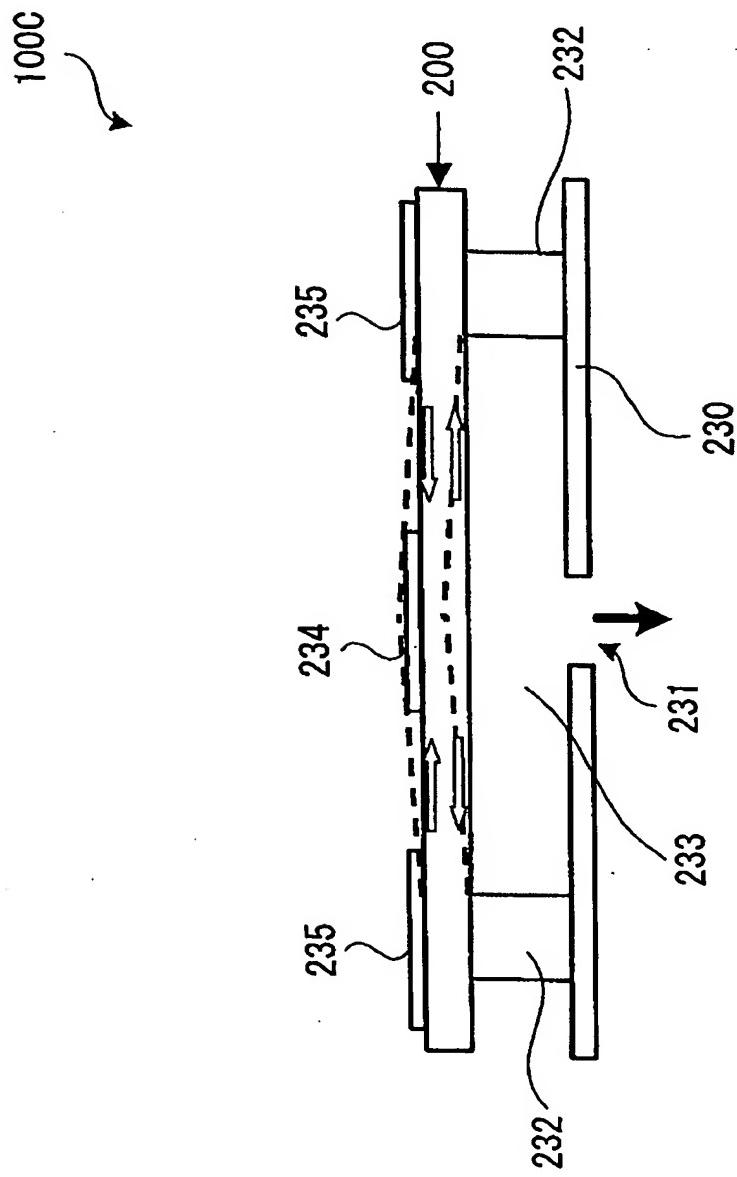


Fig. 46

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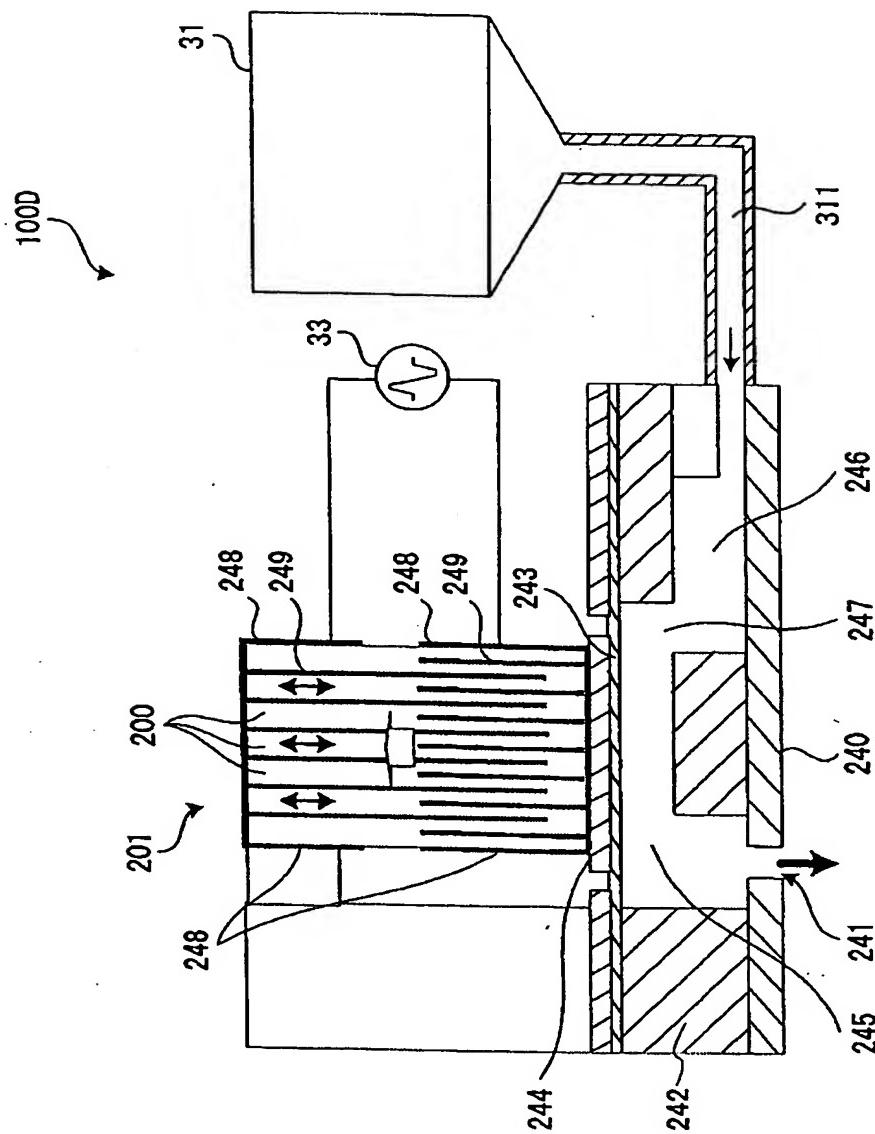


Fig. 47

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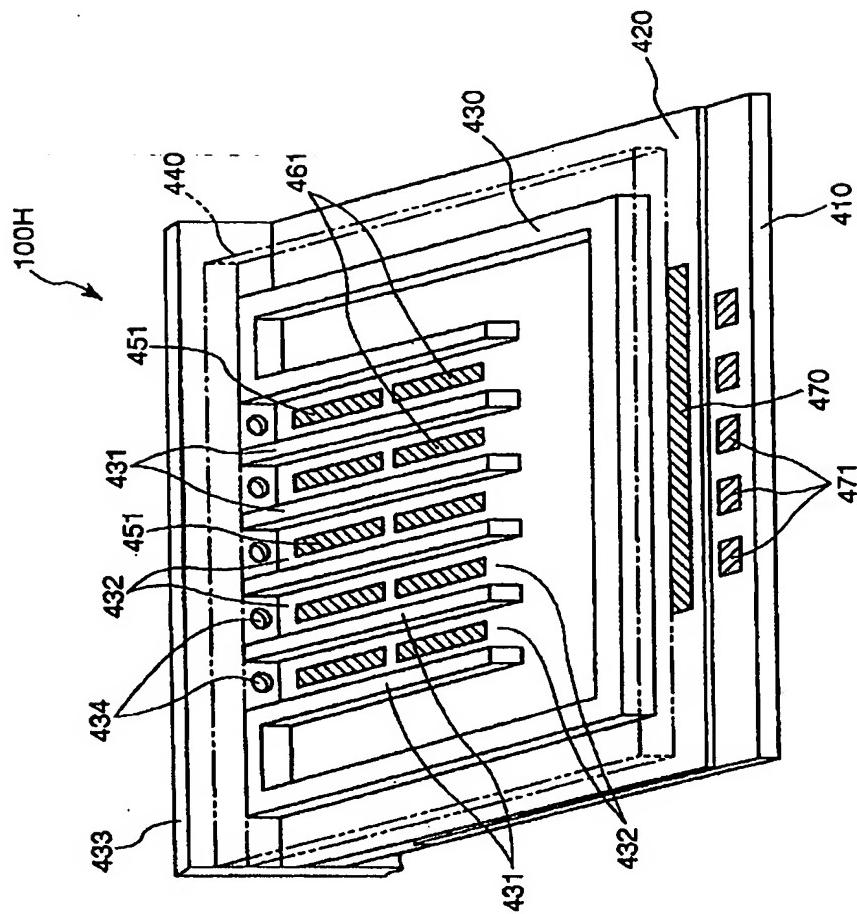


Fig. 48

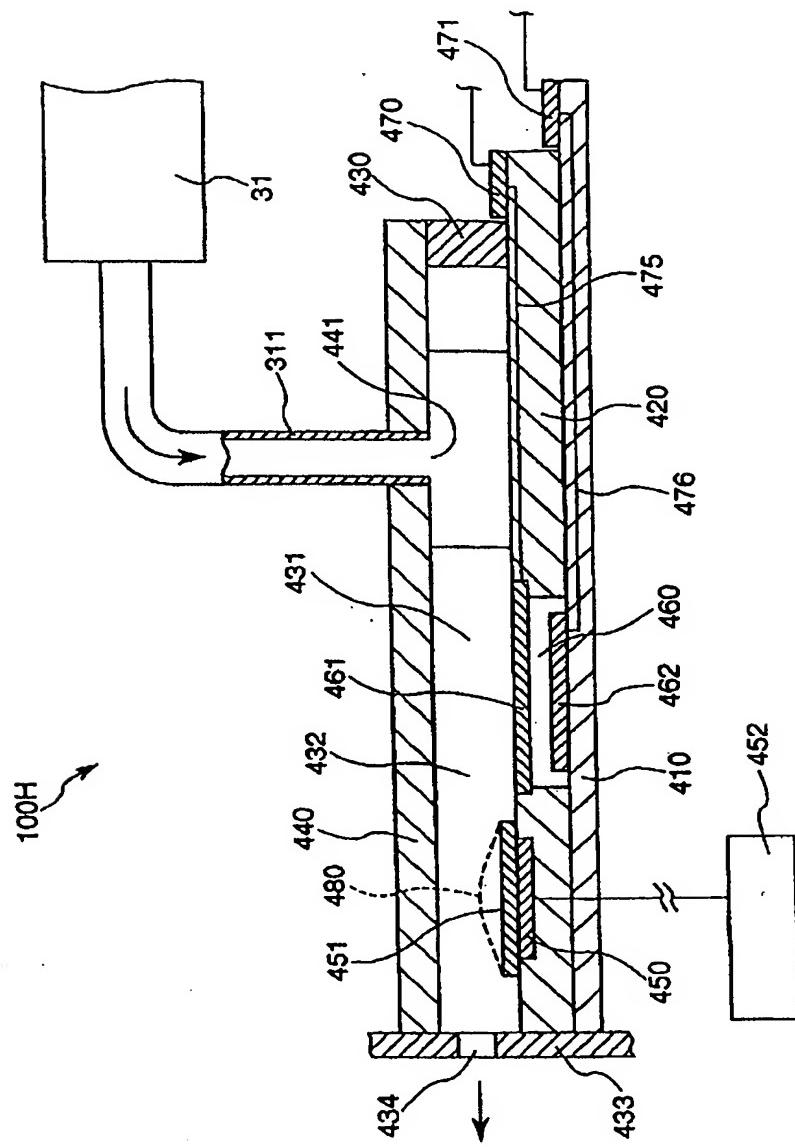


Fig. 49

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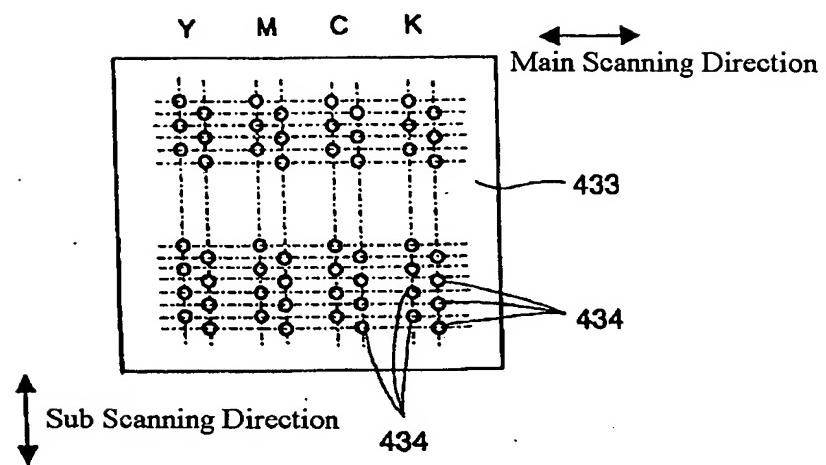


Fig. 50